

November 2nd NICO-3 Block Diagram

Project Code: 91.4CJ01.001
Raw Card: 09216-1

PCB Layer Stackup

L1:TOP
L2:GND
L3:Signal 1
L4:GND
L5: Signal 2
L6:Signal 3
L7:VCC
L8:Signal4
L9:GND
L10:BOTTOM

Battery Charger/Selector
BQ24741 58

<i>INPUTS</i>	<i>OUTPUTS</i>
<i>DOCK_PWR20_F</i>	<i>M-BAT-PWR</i>

System DC/DC
TPS51222 64

<i>VINT20</i>	<i>VCC5M</i>
	<i>VCC3M</i>

CPU DC/DC
ADP3212 65

VINT20	VCCCPUCORE
VCC1B8B	

BD3551	67
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VCC1R05LAN

<i>VCC5M_OUT</i>	<i>VCC1R05LAN</i>
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VCC1R5A

<i>VCC5M_OUT</i>	<i>VCC1R5A</i>
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VCC0R75B

MAY1510 70

<i>VCC5M_OUT</i>	<i>VCC0R75B</i>
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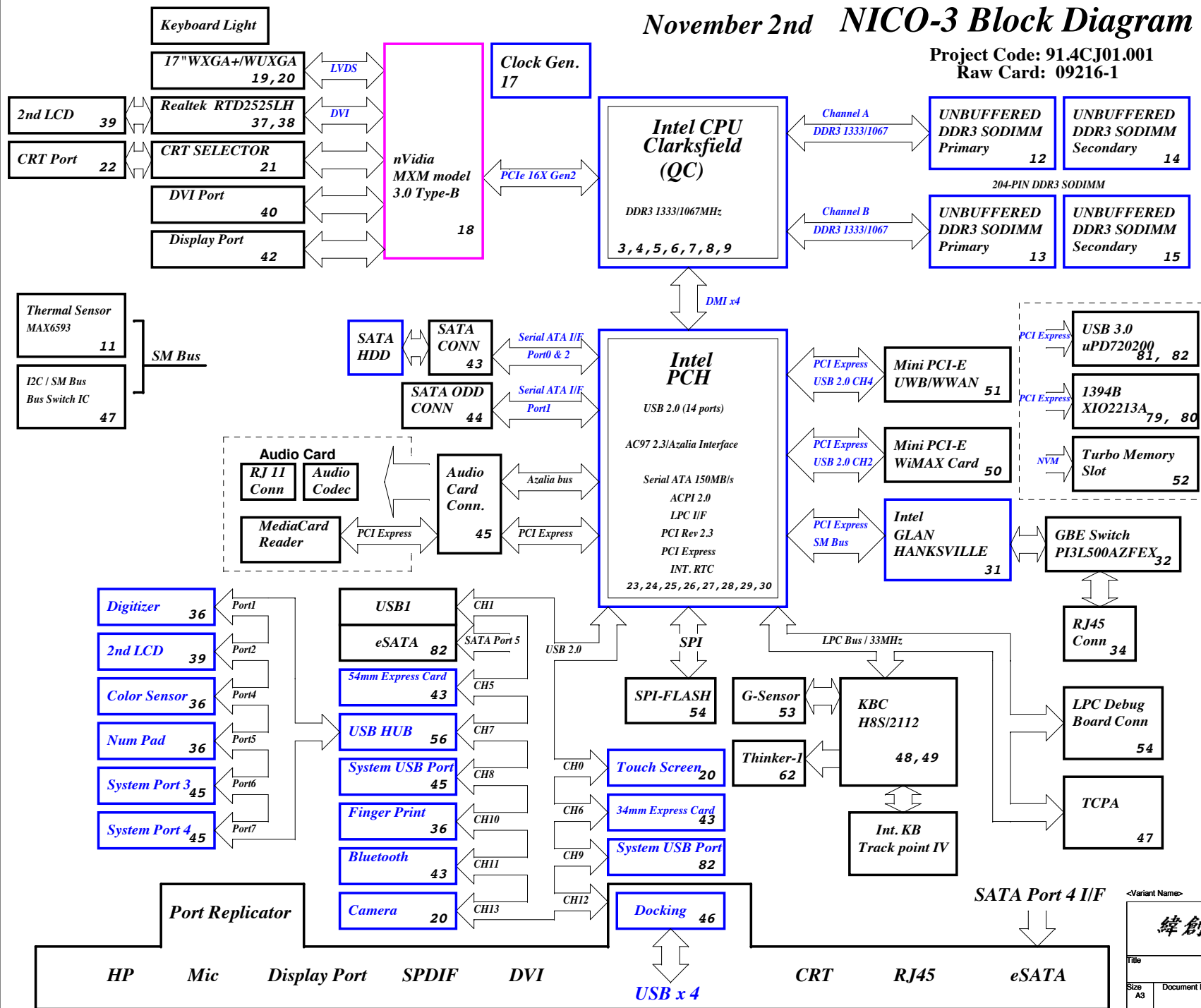
VCC1R1B_VTT
VT358 71

<i>VCC5M_OUT</i>	<i>VCC1R1B_VT</i>
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緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Block Diagram			
Size A3	Document Number		Rev
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402 => 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-0.1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 M=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

PLANAR_ID[3..0]

ICH9-M GPIO _n	39	38	37	36	Planar ID Version	Planar PCB Version
PLANAR_ID _n	3	2	1	0		
	0	0	0	0	Nico-3 Pre-DV	SA
	0	0	0	1	Nico-3 SDV	SB
	0	0	1	0	Nico-3 SIV	SC
	0	0	1	1	Nico-3 SIT	SD
	0	1	0	0	Nico-3 SVT	-1
	0	1	0	1		
	0	1	1	0		
	0	1	1	1		

EC HISTORY

[illegible]

PCI TABLE

DEVICE	IDSEL	IRQ (Default)	REQ# / GNT#
MINIPCI SLOT	AD18	F, G	REQ# 3/ GNT#
CARDBUS R5C811	AD16	SERIRQ	REQ#0 / GNT#
USB UHCI	AD29	A, C, D	
USB 2.0 EHCI	AD29	H	
DMI-to-PCI/ AC97 Modem/ AC97 Audio	AD30	B B	
LPC Bridge IDE SATA SMBus	AD31	C C B	
PCI Express	AD28	A, B, C, D	

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

[illegible]

Reference

Size
A3

Document Number

N-Note 3.0

Rev
SC

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Sheet 2

82

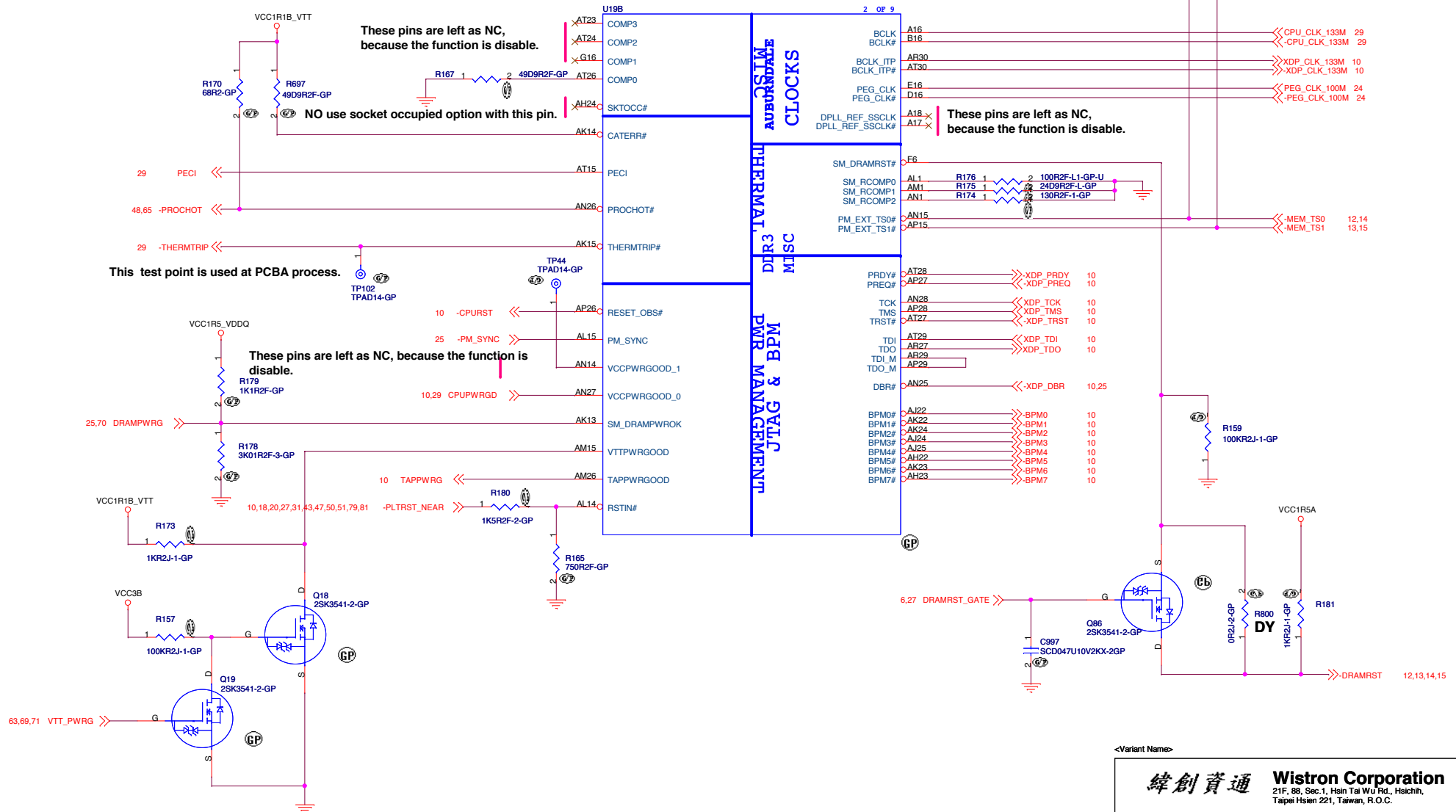
These pins are left as NC,
because the function is disable.

These Net names should be issues, because the order are not correctly.

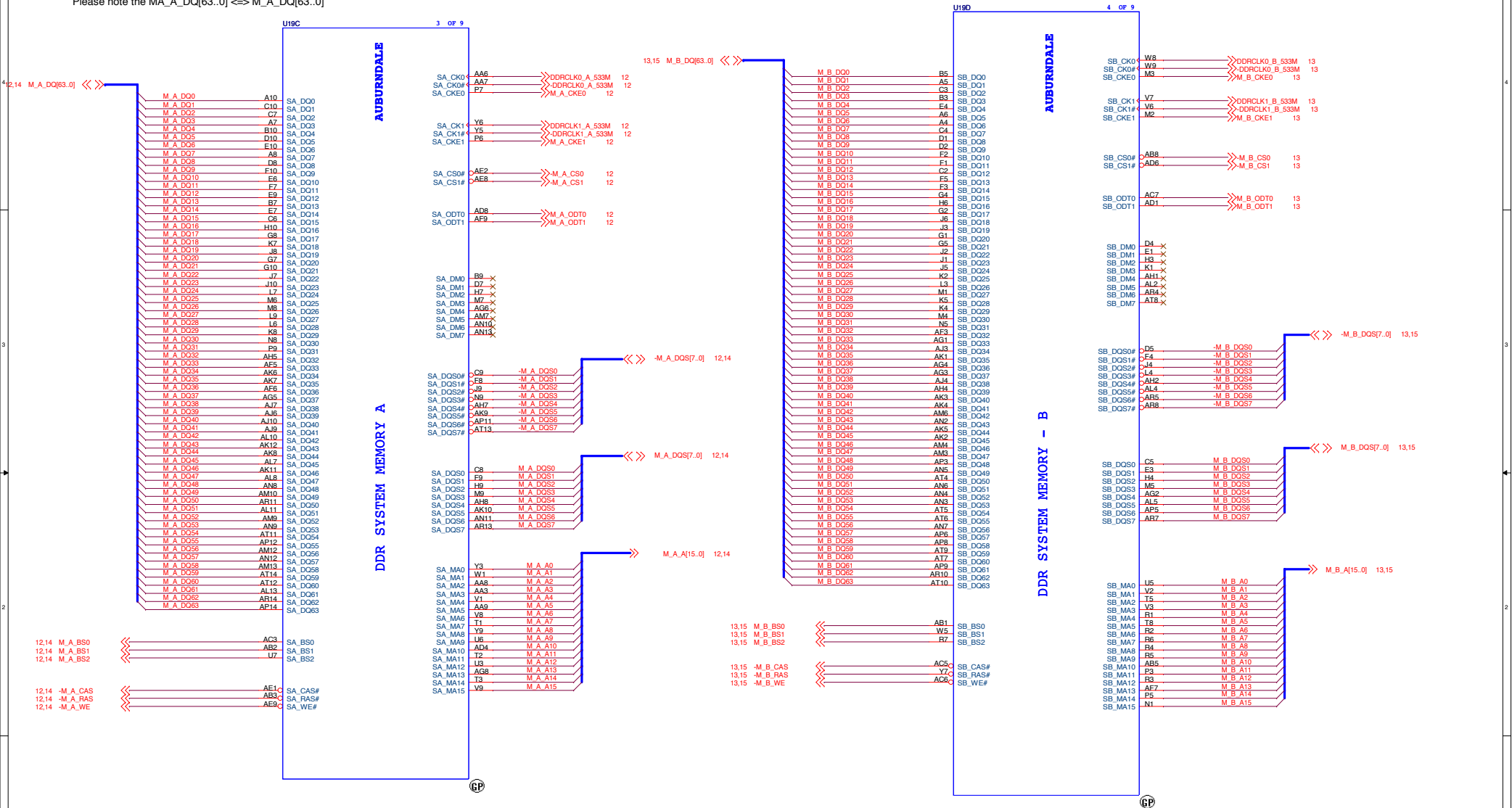
<Variant Name>			
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title ClarskField CPU(1/7):DMI/PEG/FDI			
Size A3	Document Number N-Note 3.0	Rev SC	
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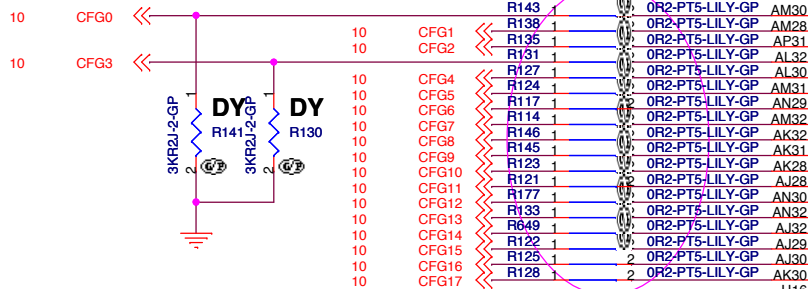
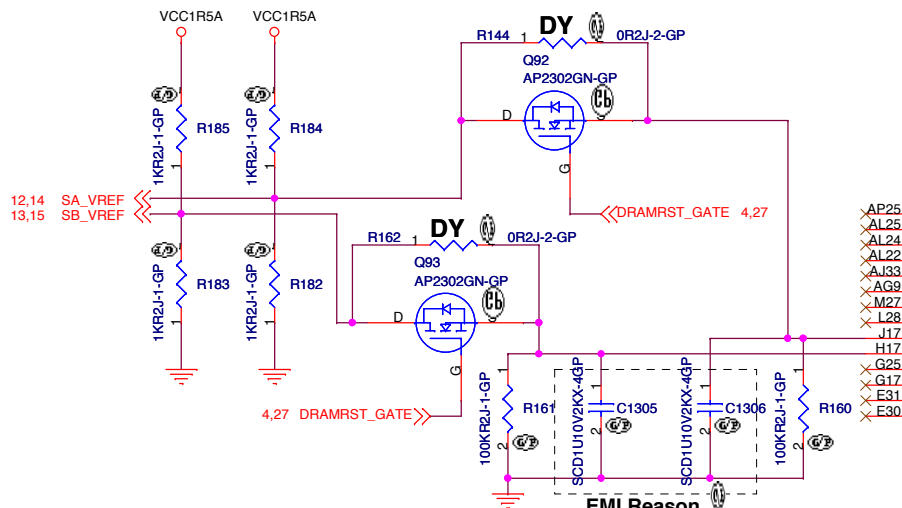
Need to refer Intel Design Guide to place CPU and route wire.

No use Catastrophic Error
Option with this pin.
Thermal Protection of CPU
at High Temp is controlled by LM26.



Please note the MA_A_DQ[63..0] <=> M_A_DQ[63..0]





SVT_EC009 10/27
Need to confirm about Internal Pullup

CFG[1:0] =>
11 : 1x16 PEG
10 : 2 x 8 PEG

CFG3 =>
1 : Normal Operation
0 : Lane Numbers Reversed.

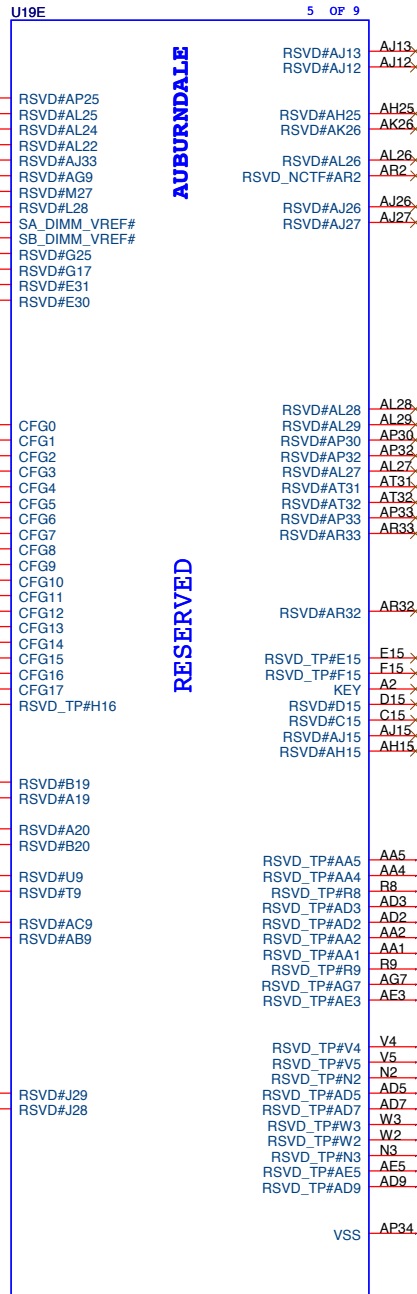
CFG[12]
This pin is left as NC,
because the GFX function is disabled.

AP25
AL25
AL24
AL22
AJ33
AG9
M27
J17
H17
G25
G17
E31
E30

CFG0
CFG1
CFG2
CFG3
CFG4
CFG5
CFG6
CFG7
CFG8
CFG9
CFG10
CFG11
CFG12
CFG13
CFG14
CFG15
CFG16
CFG17
RSVD_TP#H16

B19
A19
A20
B20
U9
T9
AC9
AB9
J29
J28

J29
J28



AUBURNDALE

RESERVED

RSVD#AJ13
RSVD#AJ12

RSVD#AH25
RSVD#AK26

RSVD#AL26
RSVD_NCTF#AR2

RSVD#AJ26
RSVD#AJ27

RSVD#AL28
RSVD#AL29

RSVD#AP30
RSVD#AP32

RSVD#AT31
RSVD#AT32

RSVD#AP33
RSVD#AR33

RSVD#AR32

RSVD_TP#E15
RSVD_TP#F15

KEY
RSVD#D15
RSVD#C15
RSVD#AJ15
RSVD#AH15

AA5
AA4
R8
AD3
AD2
AA2
AA1
R9
AG7
AE3
V4
V5
N2
AD5
AD7
W3
W2
N3
AE5
AD9

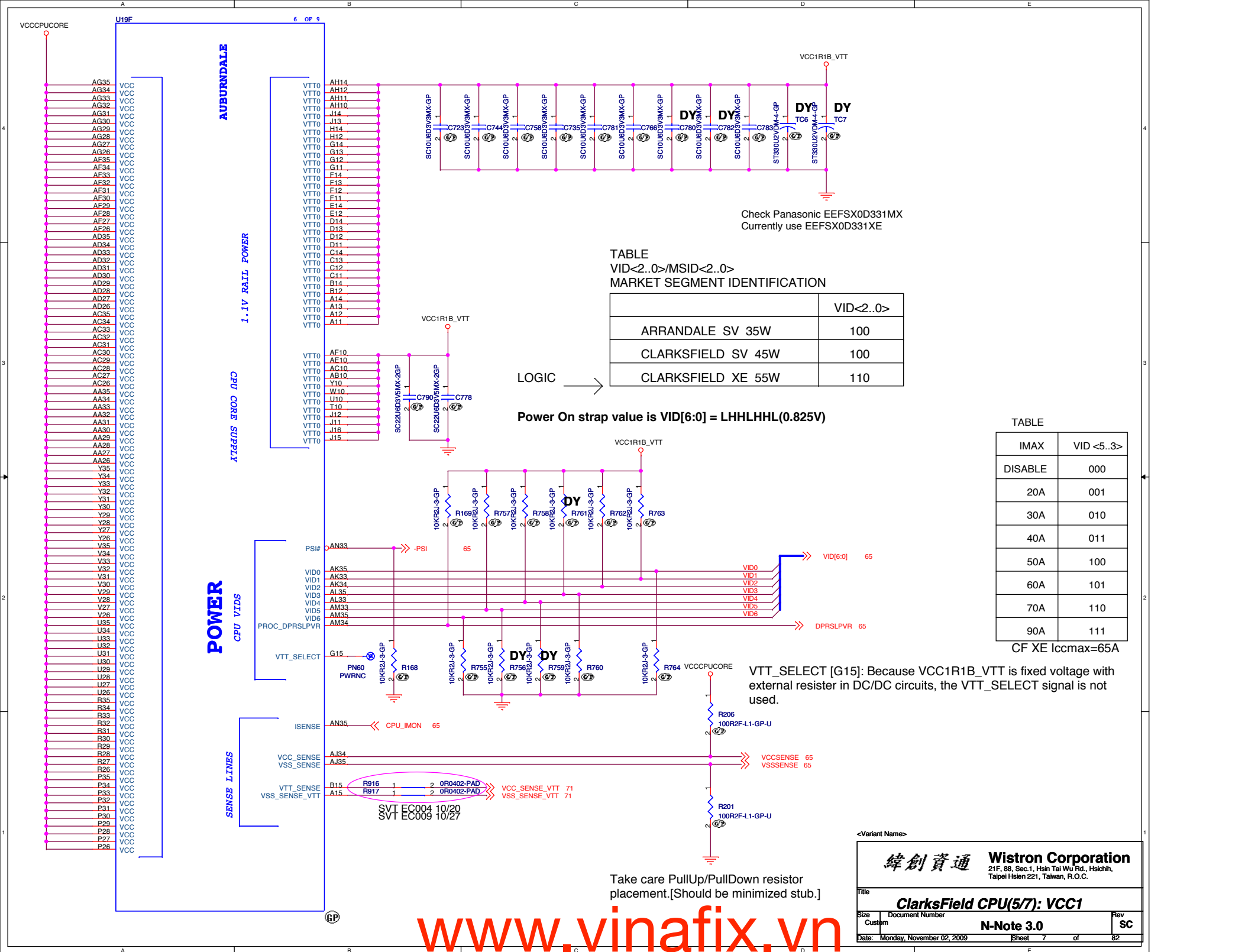
DDRCLK2_A_533M 14
-DDRCLK2_A_533M 14
M_A_CKE2 14
-M_A_CS2 14
M_A_ODT2 14
DDRCLK3_A_533M 14
-DDRCLK3_A_533M 14
M_A_CKE3 14
-M_A_CS3 14
M_A_ODT3 14
DDRCLK2_B_533M 15
-DDRCLK2_B_533M 15
M_B_CKE2 15
-M_B_CS2 15
M_B_ODT2 15
DDRCLK3_B_533M 15
-DDRCLK3_B_533M 15
M_B_CKE3 15
-M_B_CS3 15
M_B_ODT3 15

RSVD_TP#V4
RSVD_TP#V5
RSVD_TP#N2
RSVD_TP#AD5
RSVD_TP#AD7
RSVD_TP#W3
RSVD_TP#W2
RSVD_TP#N3
RSVD_TP#AE5
RSVD_TP#AD9

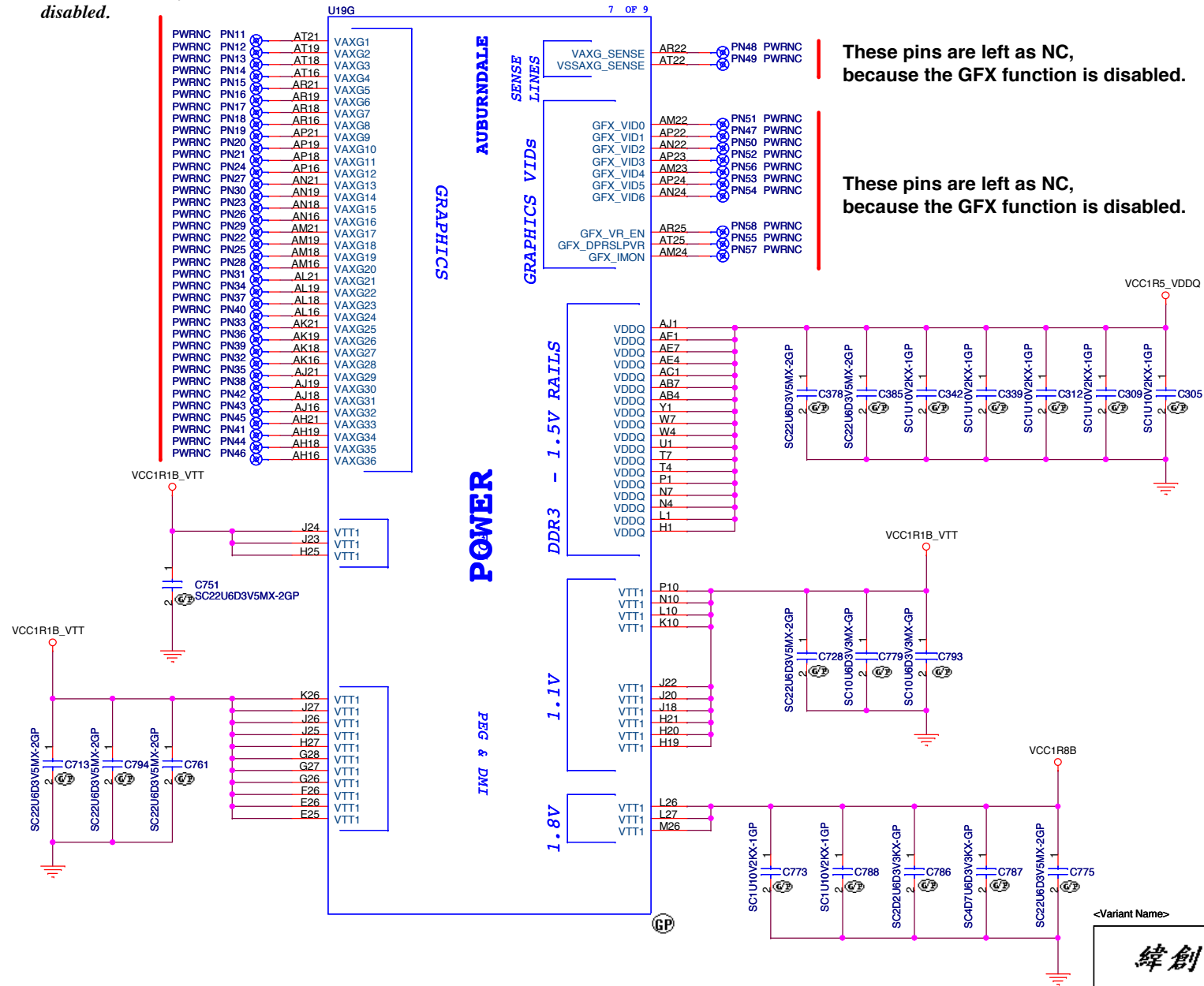
VSS

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ClarksField CPU(4/7): CFG/RSVD			
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These pins should be left as NC,
because the GFX function is
disabled.

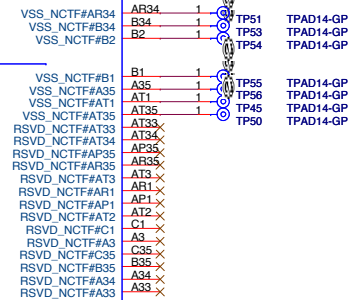
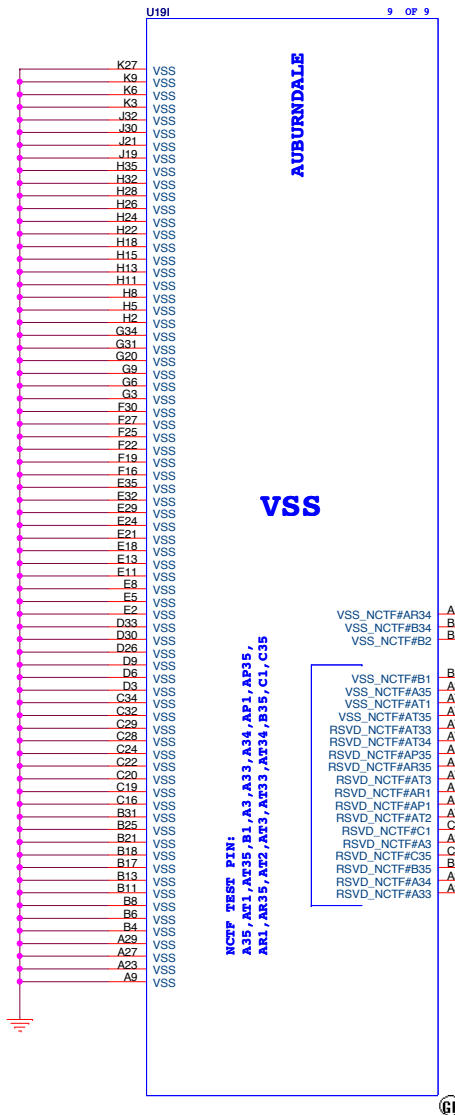
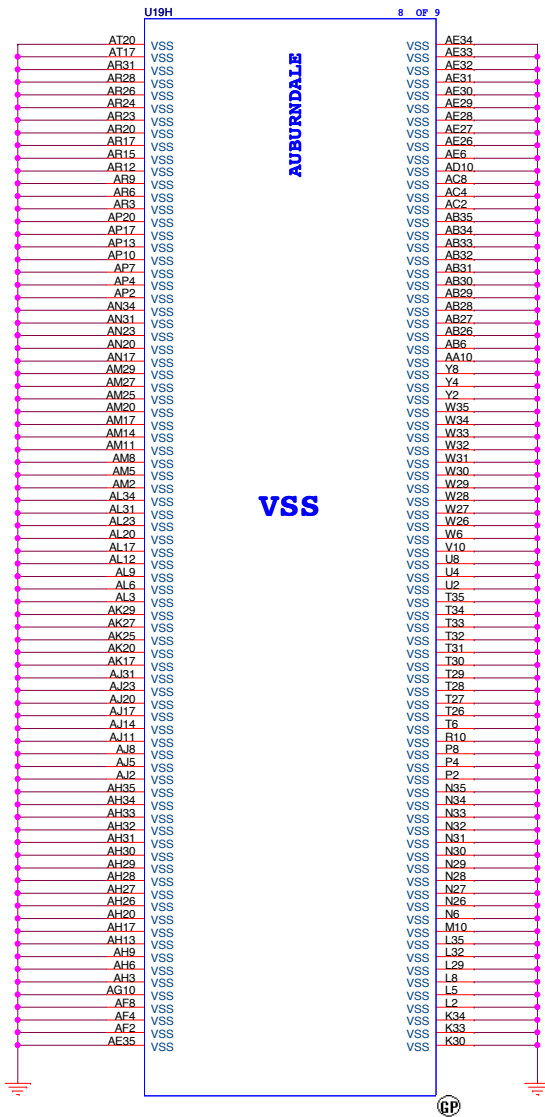


These pins are left as NC,
because the GFX function is disabled.

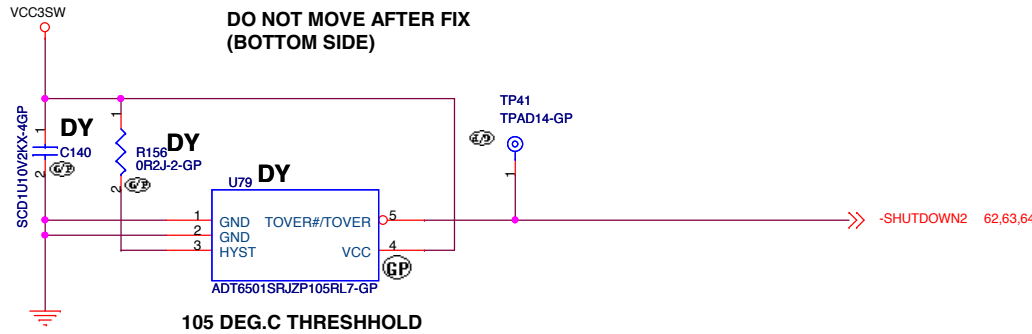
These pins are left as NC,
because the GFX function is disabled.

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ClarksField CPU(6/7): VCC2			
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Thermal Sensor for CPU



[Source Candidate]

		U9	R156
1	ADI	ADT6501SRJZP105RL7	ASM
2	MAXIM	MAX6501UKP105+1	ASM
3	MAXIM	MAX6519	NO_ASM
4	ROHM	BDE1055G	NO_ASM

**THESE CAPS MUST BE PLACED AS
CLOSE AS POSSIBLE TO MAX6593**

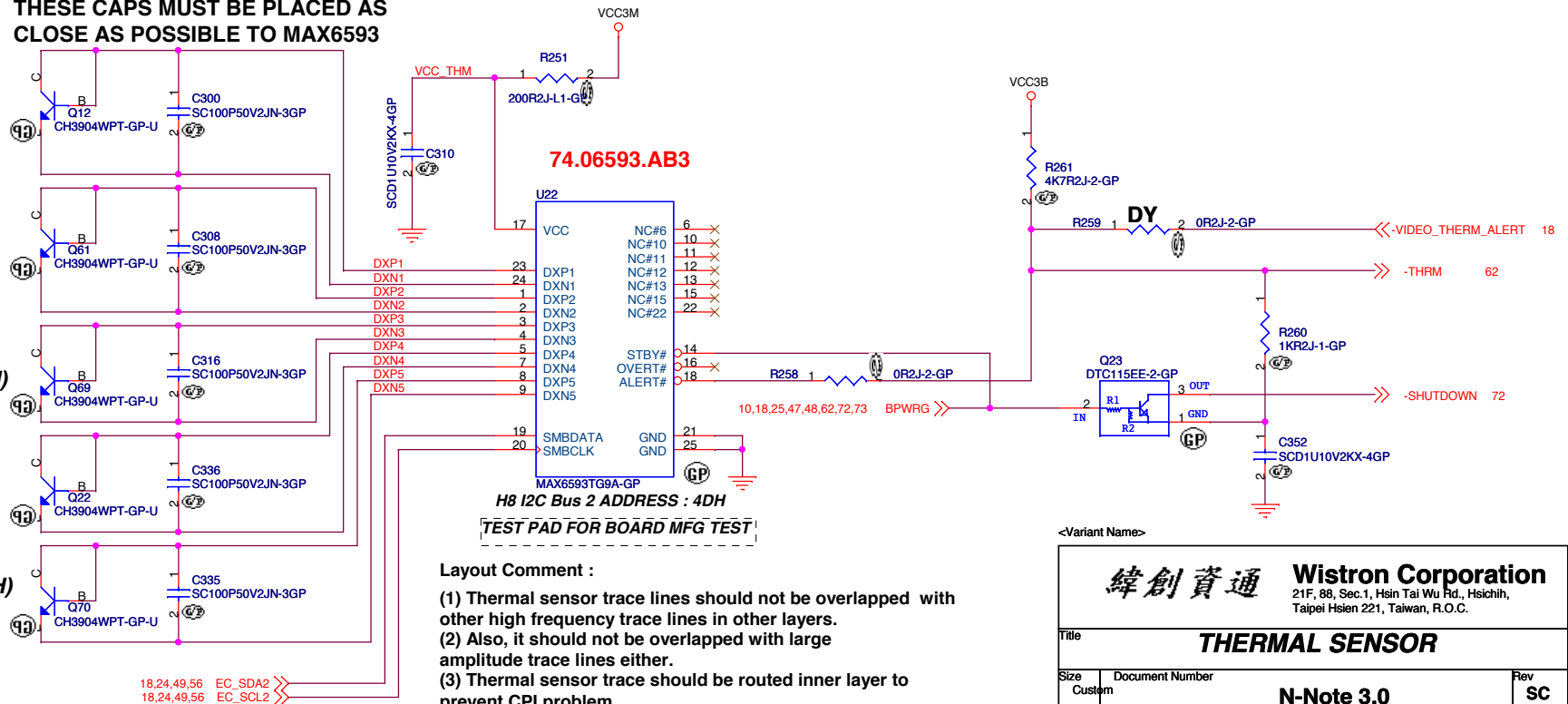
TO WLAN(TOP)

TO GBE

TO MEMORY(BOTTOM)

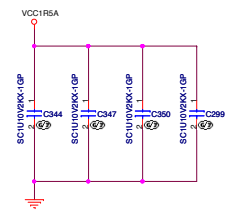
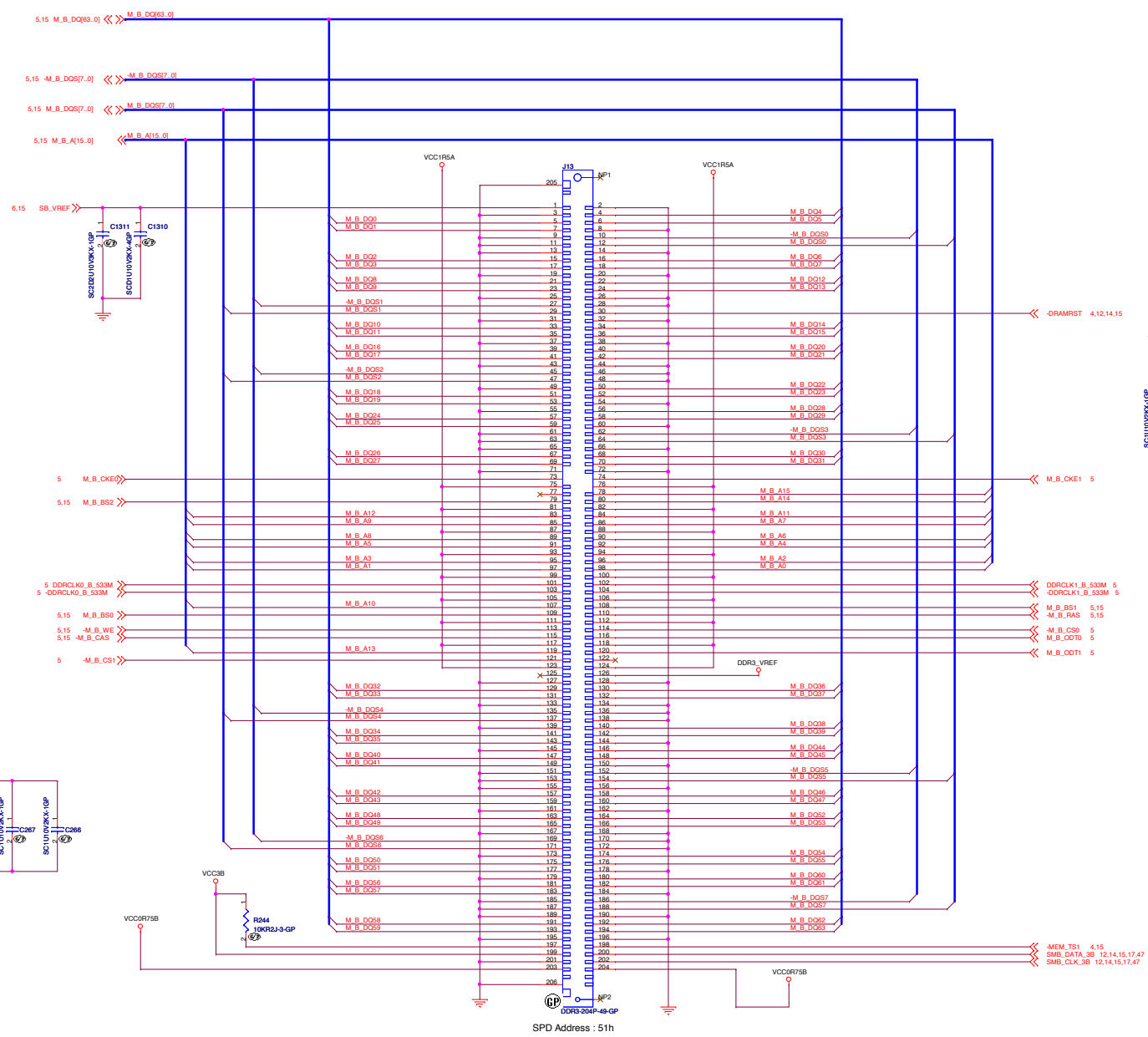
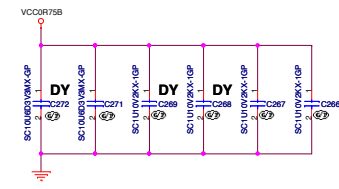
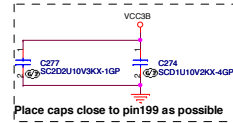
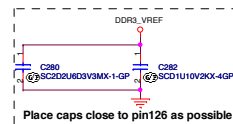
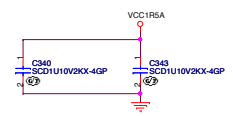
TO CPUCORE FET

TO BASE COVER (PCH)



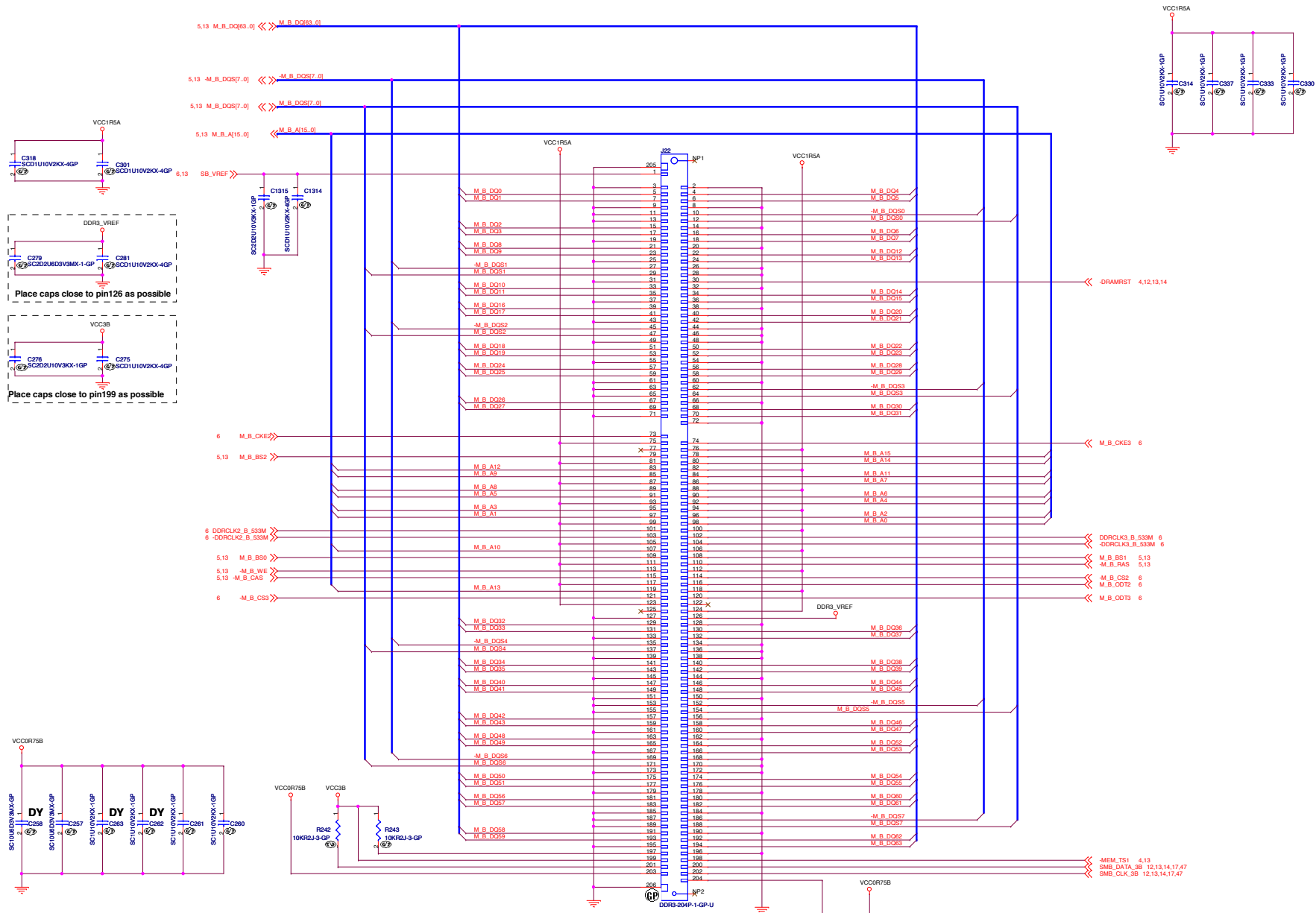
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
THERMAL SENSOR	
Size Custom	Document Number N-Note 3.0
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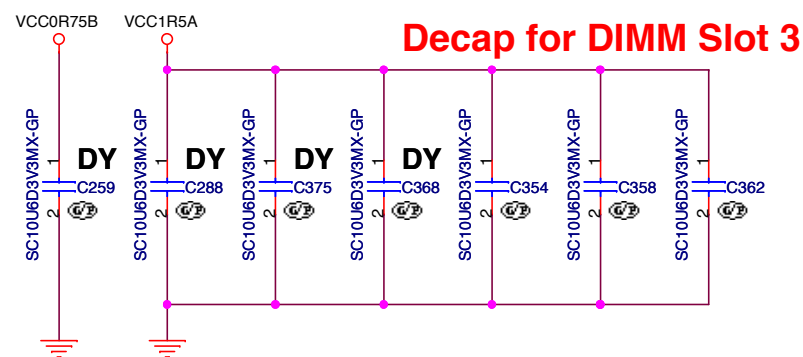
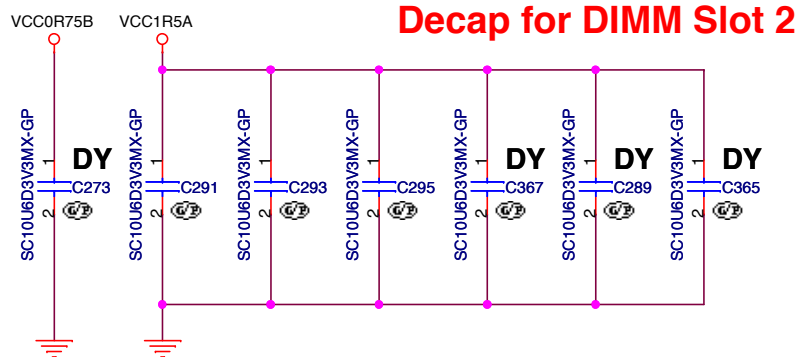
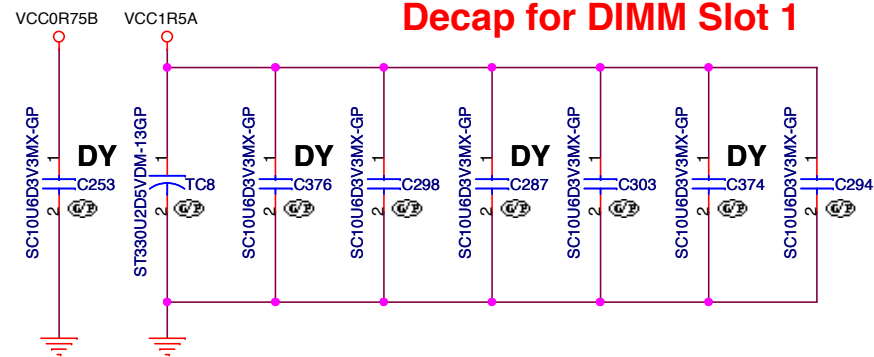
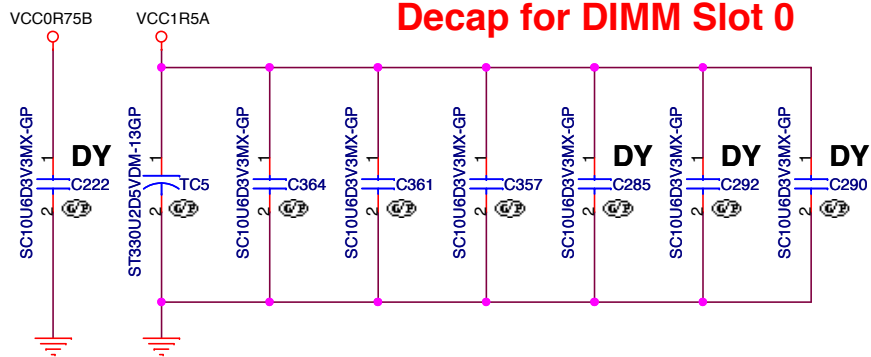
This connector should be placed on far side from CPU.
H=5.2mm

<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 321, Taiwan, R.O.C.</div> </div>			
File	DDR3 SODIMM CH-B Primary		
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SPD Address : 53h
 This connector should be placed on near side from CPU.
 bom change to 62.10017.M11 (9/2)

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<div> <div>21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.</div> </div>			
File	DDR3 SODIMM CH-B Secondary		
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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DECAP For DIMMs

Size
A4

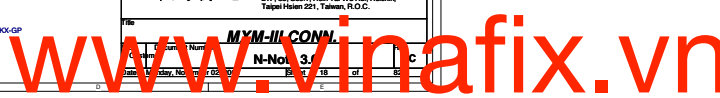
Document Number

N-Note 3.0

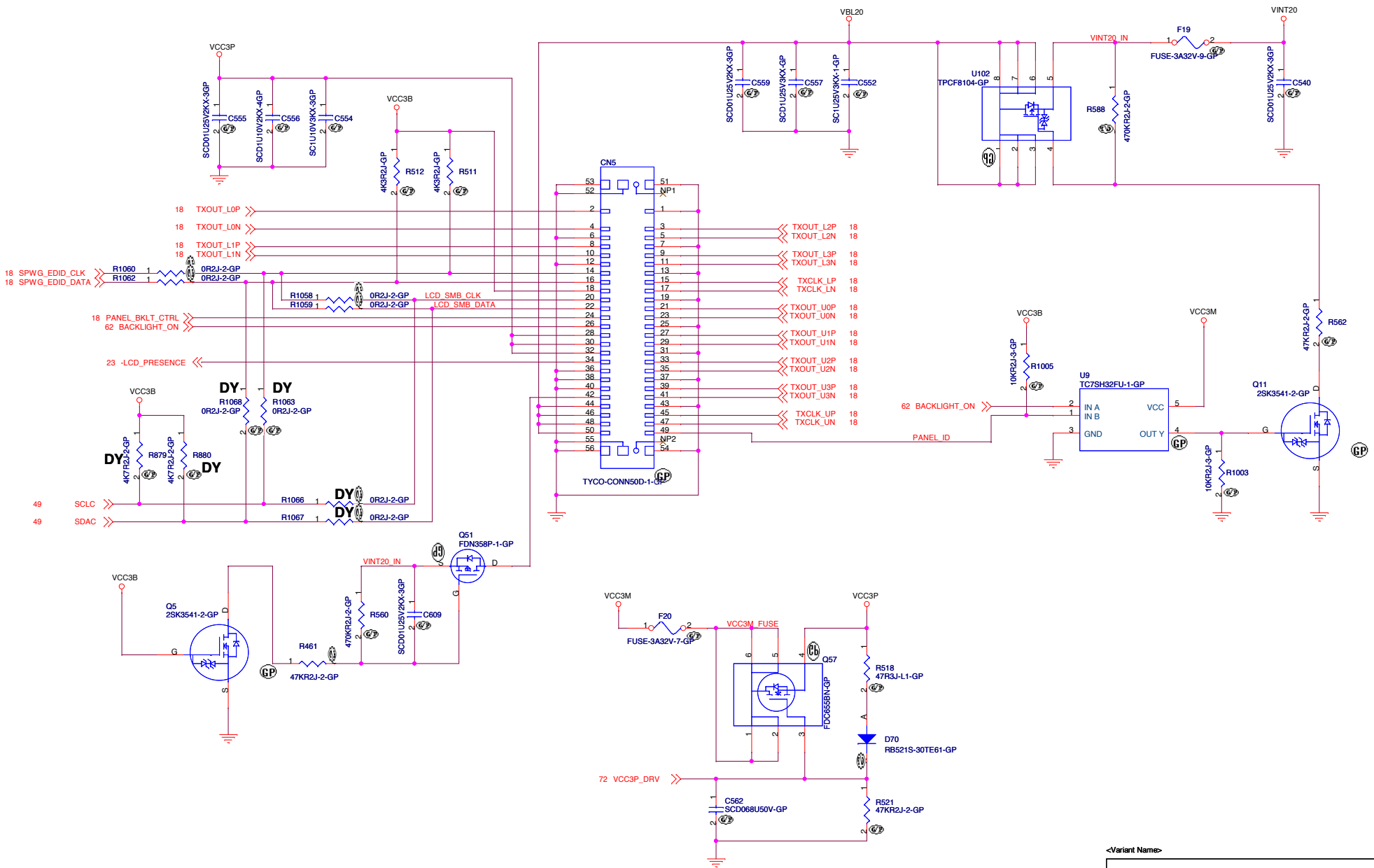
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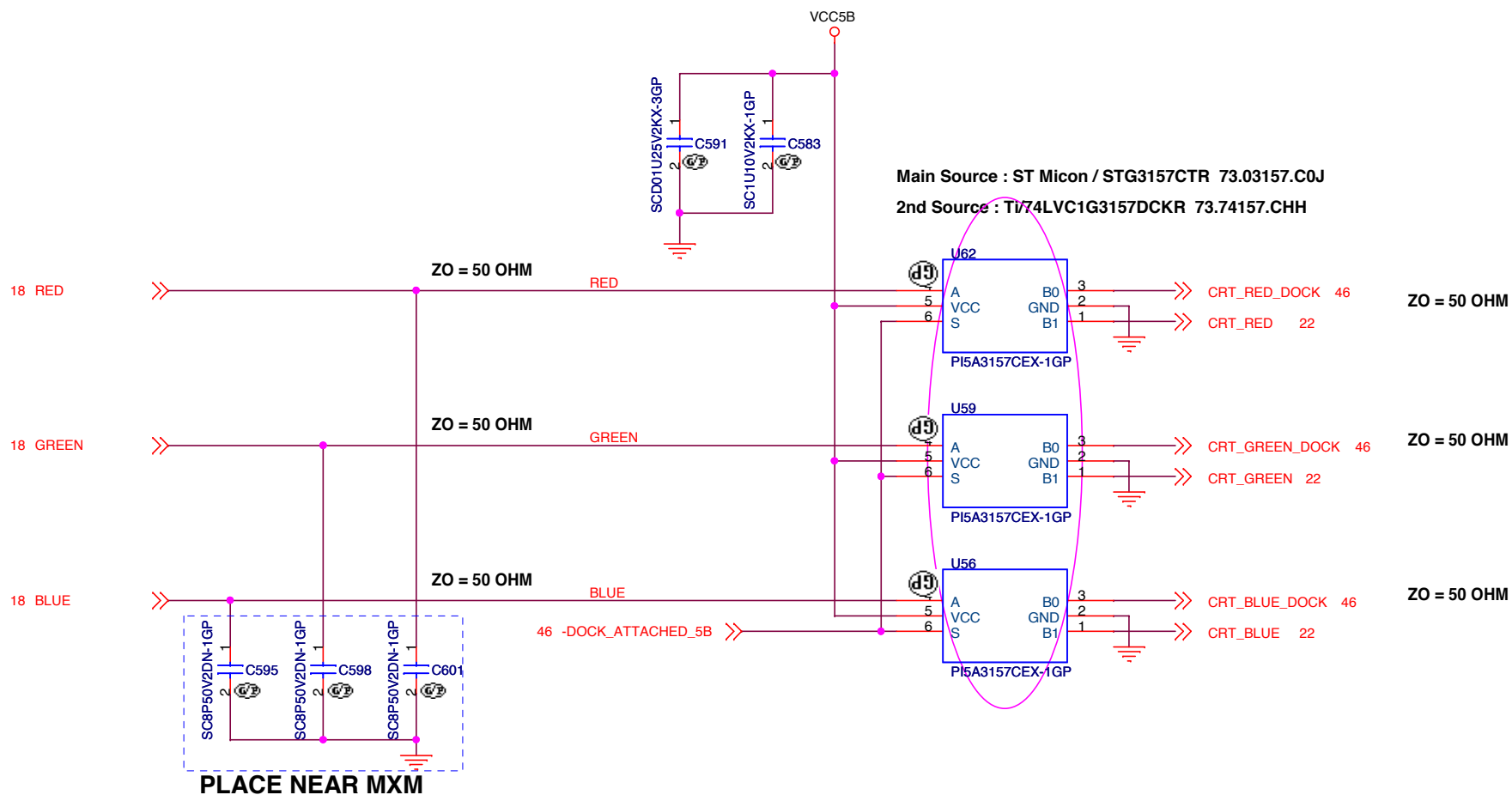


I/O#	Signal	IN/OUT	Description
I/O0	-NV_2ND_DDC_EN	OUT	0: DDC for 2nd LCD 1: DDC for System DVI
I/O1	PANEL_STATUS	IN	not used 0: 2nd LCD Lid Close 1: 2nd LCD Lid Open
I/O2	-NV_2ND_EN	OUT	0: DVI_A to 2nd LCD 1: DVI_A to System DVI



<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD CONNECTOR			
Size A3	Document Number	N-Note 3.0	Rev SC
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緯創資通

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Title

CRT SELECTOR

Size
 A4

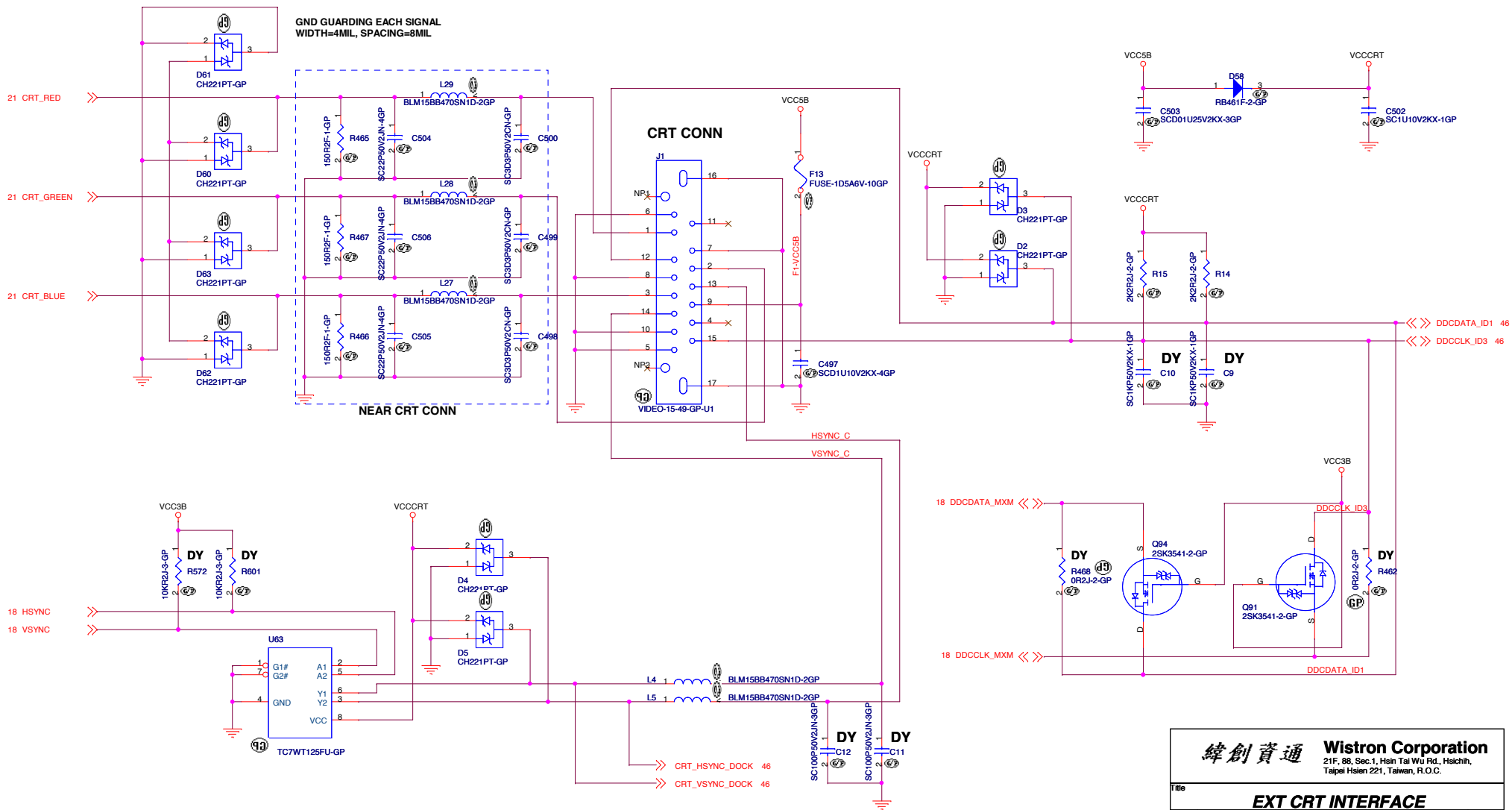
Document Number

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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
EXT CRT INTERFACE			
Size	Document Number	Rev	
Custom		SC	
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INTVRMEM pin should have pull up resistor to enable integrated 1.05V VRM.

HDA_SYNC has a weak[20K] internal pull down. 45 ACZ_BCLK_ADI
The pin is low, 1.8V is provided by on die PLL VR.
The pin is high, 1.5V is provided by on die PLL VR.

HDA_BCLK has a weak(20K) internal pull down.

HDA_RST# has a weak(20K) internal pull down.

HDA_SDIN[3:0] has a weak(20K) internal pull down.

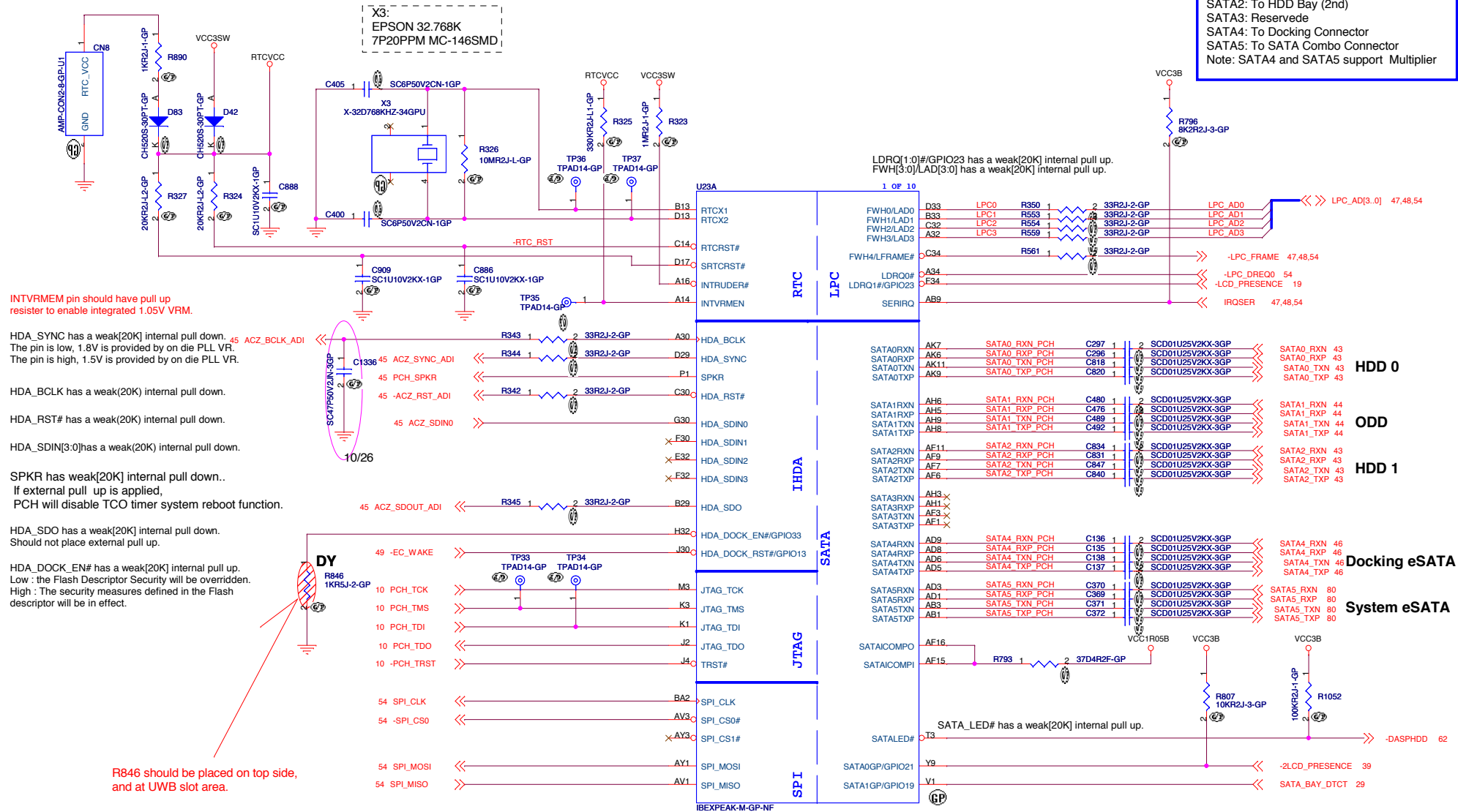
SPKR has weak[20K] internal pull down..
If external pull up is applied,
PCH will disable TCO timer system reboot function.

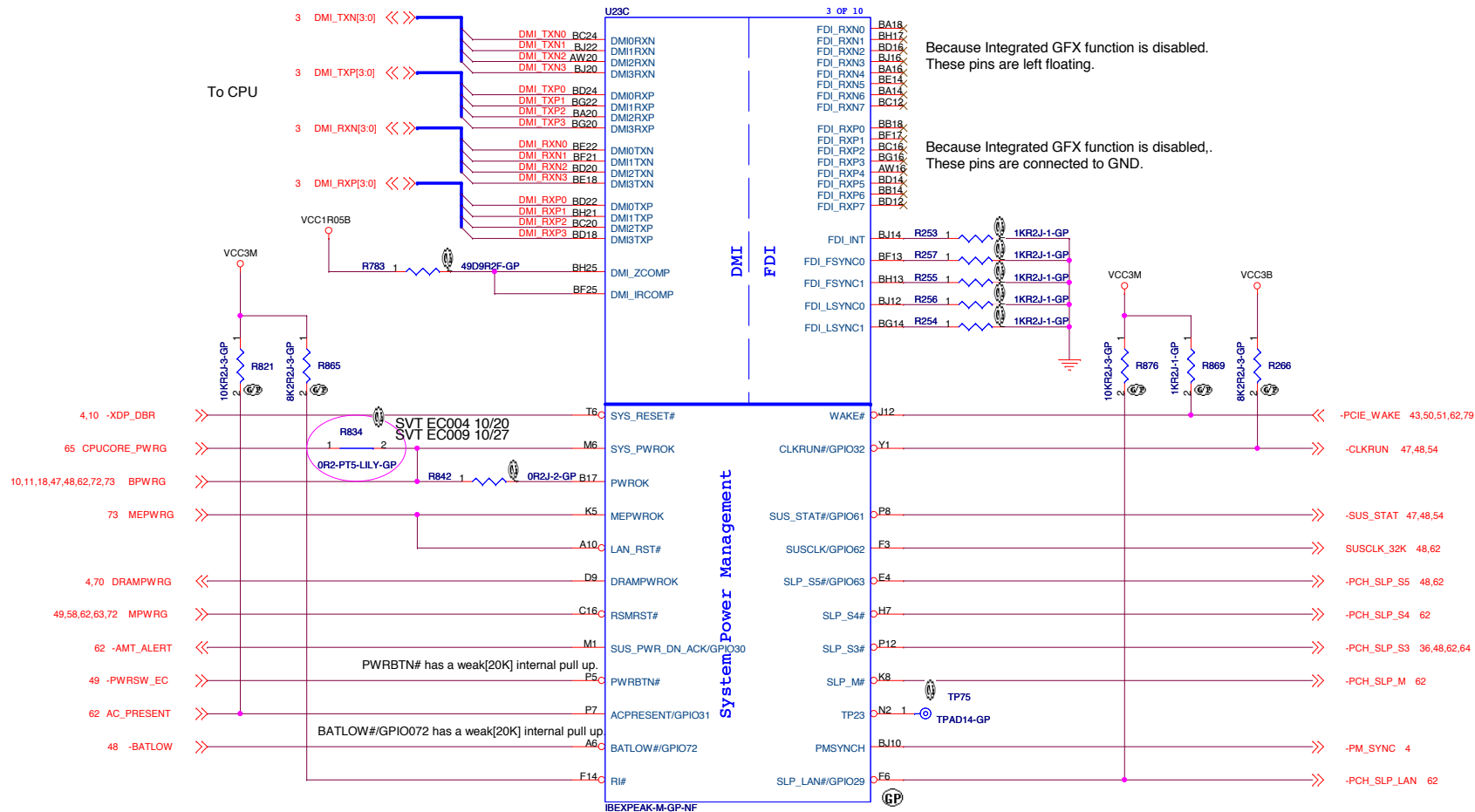
HDA_SDO has a weak[20K] internal pull down.
Should not place external pull up.

HDA_DOCK_EN# has a weak[20K] internal pull up.
Low : the Flash Descriptor Security will be overridden.
High : The security measures defined in the Flash descriptor will be in effect.

R846 should be placed on top side,
and at UWB slot area.

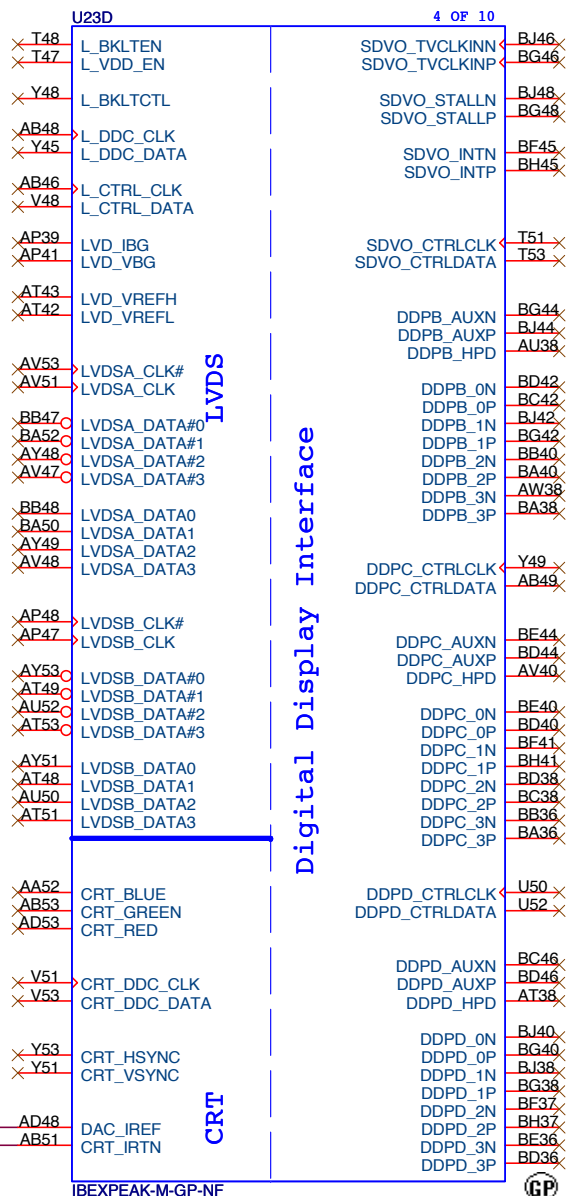
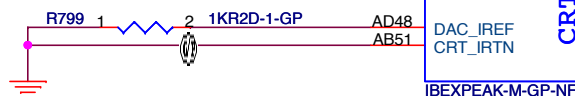
SATA0: To HDD Bay
SATA1: To ODD Bay
SATA2: To HDD Bay (2nd)
SATA3: Reserved
SATA4: To Docking Connector
SATA5: To SATA Combo Connector
Note: SATA4 and SATA5 support Multiplier





L_DDC_DATA has a weak[20K] internal pull down.

Because Integrated GFX function is disabled,
These pins are left floating.



Digital Display Interface

SDVO_CTRLCLK/SDVO_CTRLCLK has a weak[20K] internal pull down.

Because Integrated GFX function is disabled,
These pins are left floating.

DDP[D:C]_CTRLCLK has a weak[10K] internal pull down.
DDP[D:C]_CTRLDATA has a weak[20K] internal pull down.

<Variant Name>

緯創資通

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Title

PCH (4/8):LVDS/CRT/DDI

Size
A4

Document Number

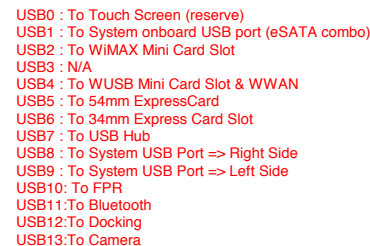
N-Note 3.0

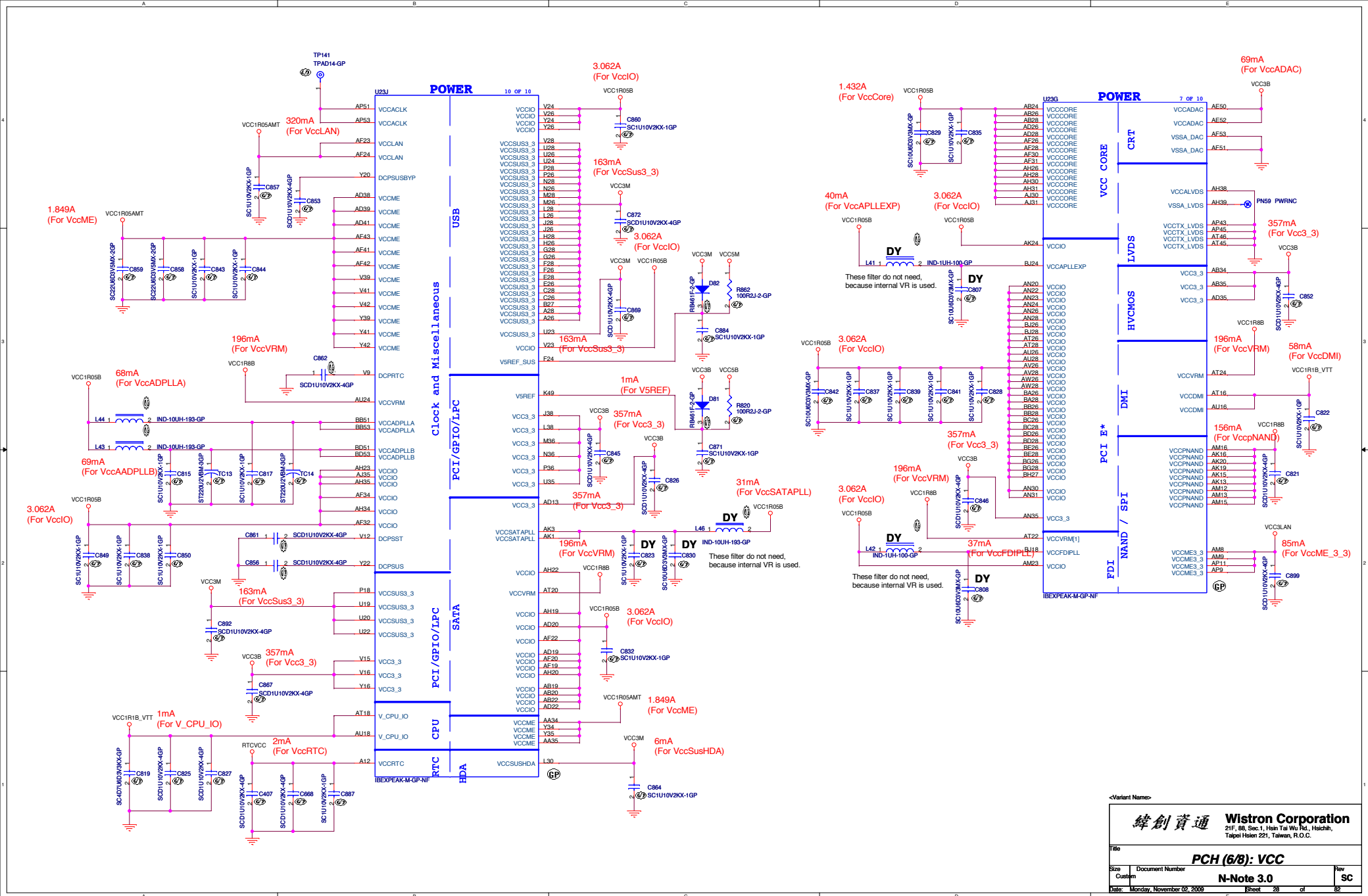
Rev
SC

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GNT0# has a weak[20K] internal pull up.
GNT1#/GPIO1 has a weak[20K] internal pull up.
To use SPI/IF flash BIOS, GNT1#/GPIO1
and GNT0# should not place external pull down.
GNT2#/GPIO53 has a weak[20K] internal pull up.
This pin should not have external pull down.
GNT3#/GPIO55 has a weak[20K] internal pull up.
If external pull down is applied,
PCH will be "tomblock swap" mode.



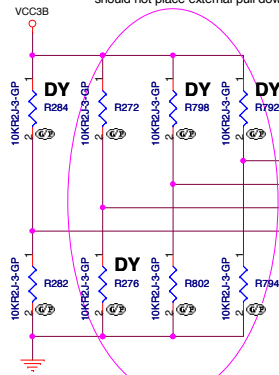


GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull down/up.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

For LAN PHY Power Control

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



SVT_EC003 10/19

External Pull Up requires for PCIECLKREQ# lines.

For Solder crack detection.

TACH[3:0] has internal pull up.
49 -EC_SCI >>>

43 HDD_SUBCARD_ID0 >>>
43 HDD_SUBCARD_ID1 >>>

31 LANPHYPC <<<

TPAD14-GP TP74 <<<

TPAD14-GP TP110 <<<

23 SATA_BAY_DTCT <<<
To use for SATA Bay detection

46,56 VCC3_USBHUB_PWRON <<<

SATACLKREQ#/GPIO35 pin is
set to output mode[Low] at Reset.

PLANARID0 <<<

PLANARID1 <<<

PLANARID2 <<<

PLANARID3 <<<

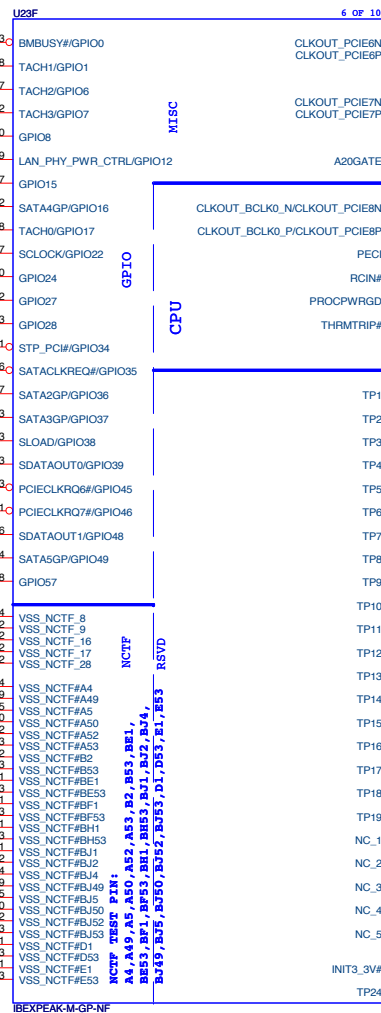
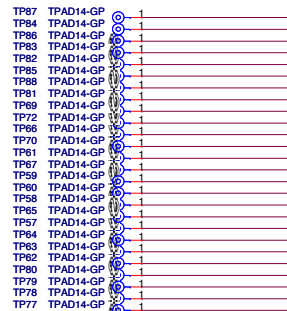
43 -CLKREQ_EXC2 >>>

79 -CLKREQ_USB30 >>>

43 -BDC_PRESENCE >>>

47 -DTPM_PRESENCE >>>

External Pull Up requires for PCIECLKREQ# lines.



These pins are left as NC.

INIT3_3V# has a weak[20K] internal pull up.

To 54mm ExpressCard Slot

To USB 3.0 Controller

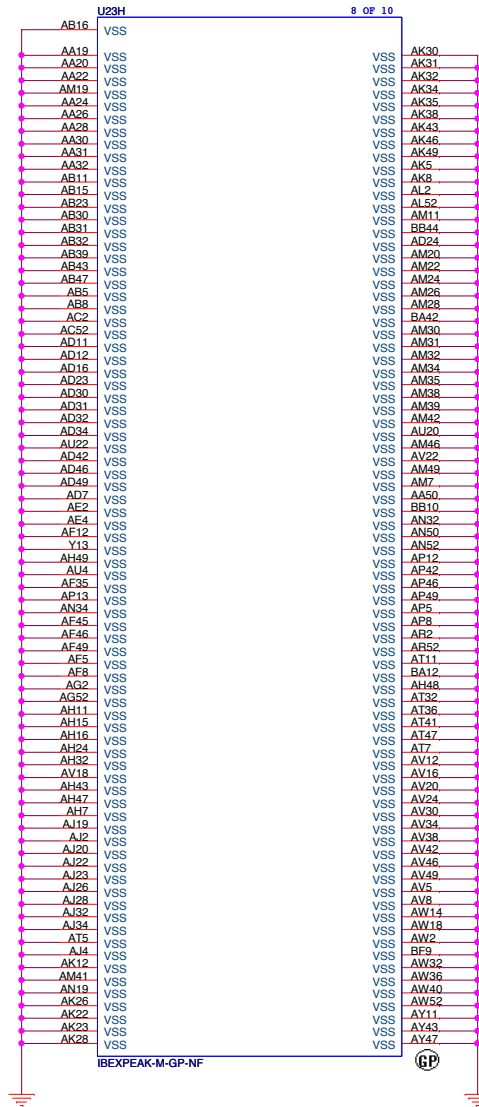
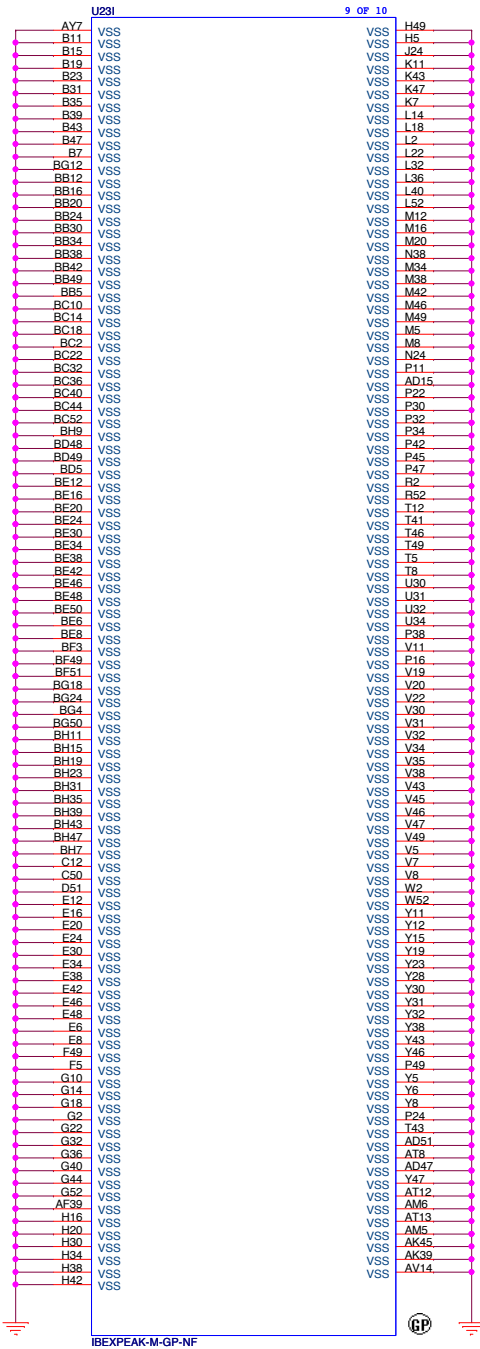
From H8

To CPU

From/To CPU (Single wire bus,
For Thermal Management)
From H8 (CPU Reset by H8)
To CPU Powergood pin

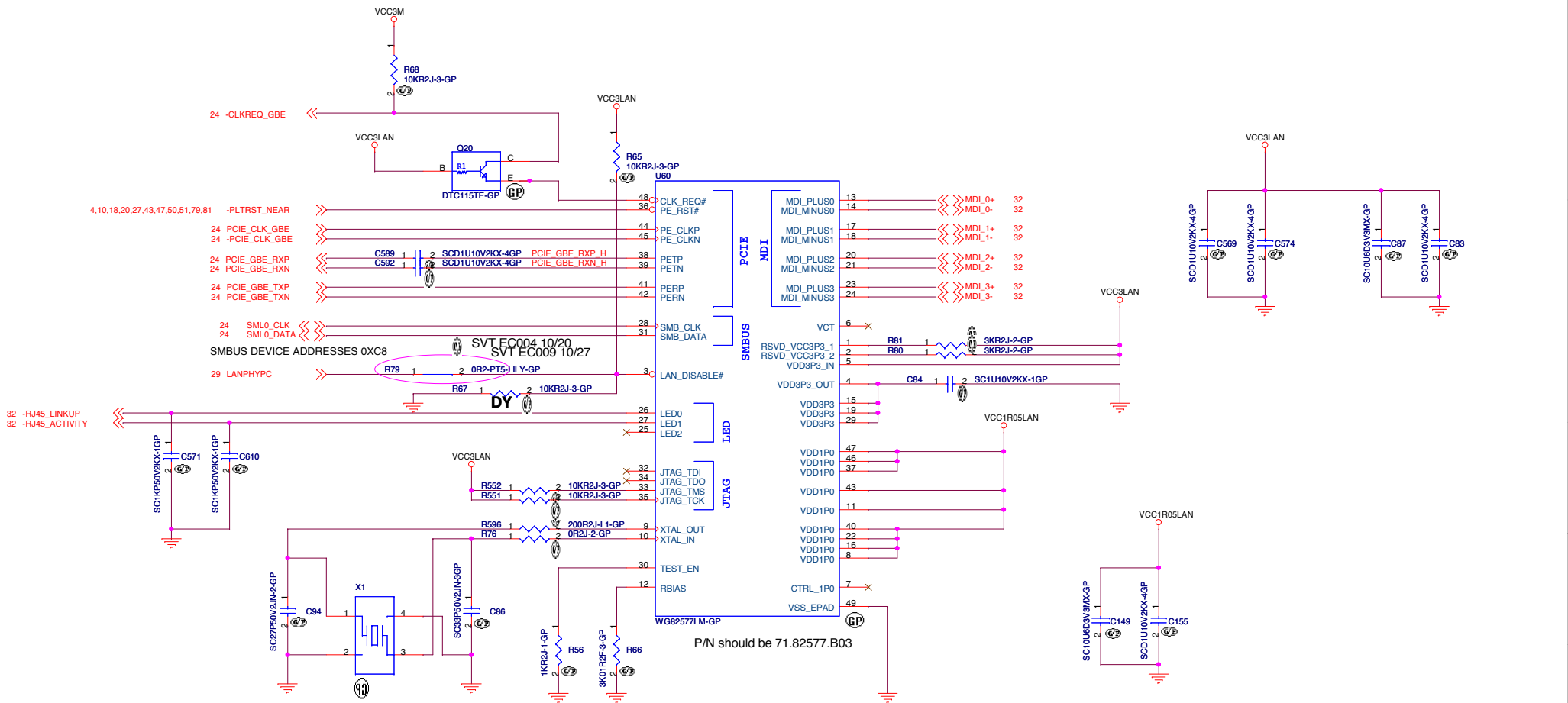
<Variant Name>

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Haichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH (7/8):GPIO/NTCF/RSVD	
Size Custom	Document Number N-Note 3.0
Date Monday, November 02, 2009	Sheet 29 of 82



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
PCH (8/8):GND		
Size	Document Number	Rev
A3		SC
Date:	Monday, November 02, 2009	Sheet 30 of 82



R82/0-ohm was changed to C956/10pF in EC.
(nico3-sb_0212_p31_0217.pdf)

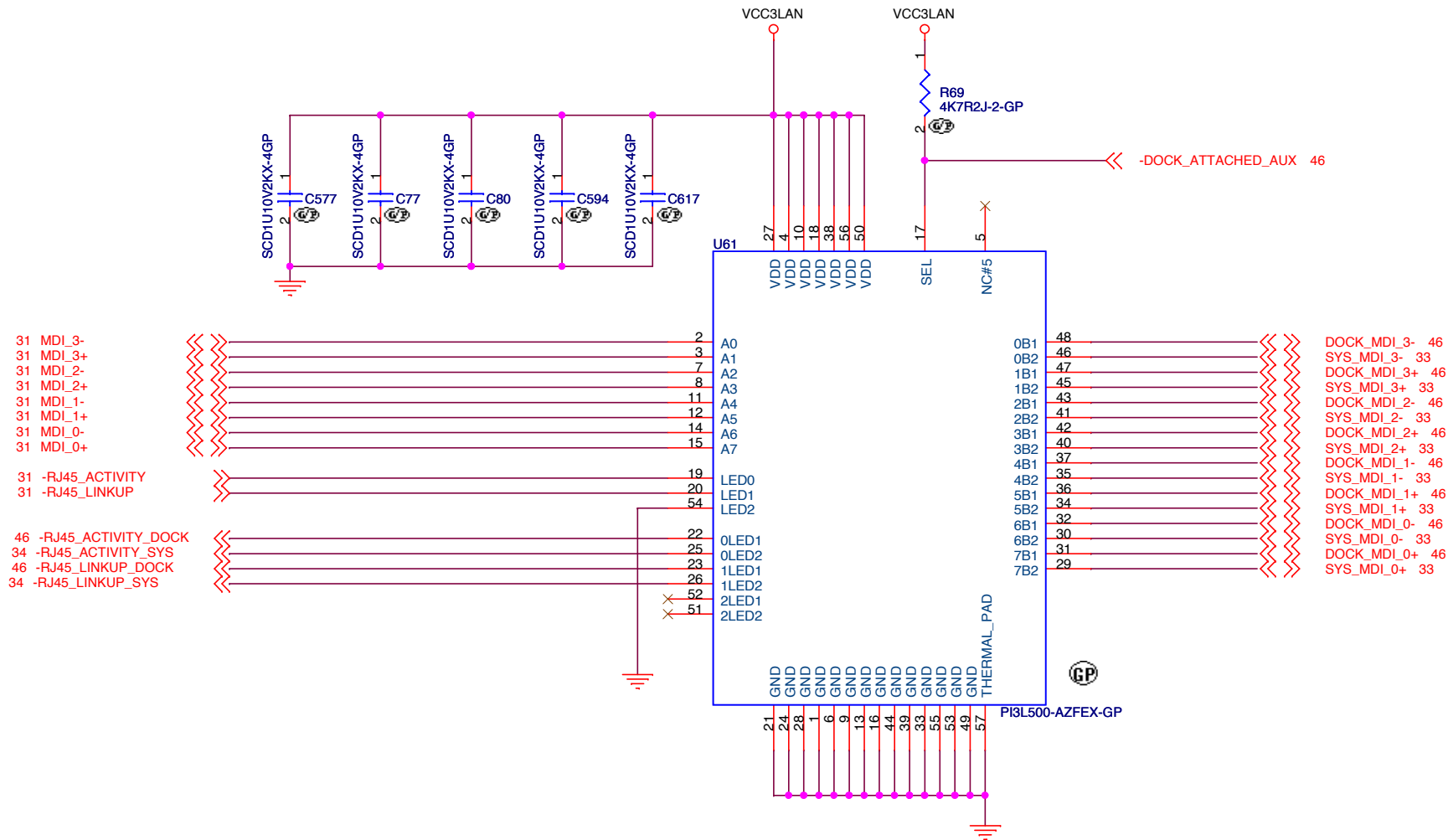
X1:
KDS 25M 18P30PPM DSX321G SMD

(Intel validated version is "DSX321G-25.000M-18pF-30-30R2")
KDS P/N= 1B225000CC0N
TXC P/N= 7V25020001
KDS TWN confirmed that "1B225000CC0N" is the same as "1C225000CC0M".
2008/11/26

NOTE: VCC1R05LAN WILL WORK AT 0.95V TO 1.15V

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		GBE HANKSVILLE	
Size	Document Number	N-Note 3.0	
A3		Rev SC	
Date: Monday, November 02, 2009		Sheet 31 of 82	

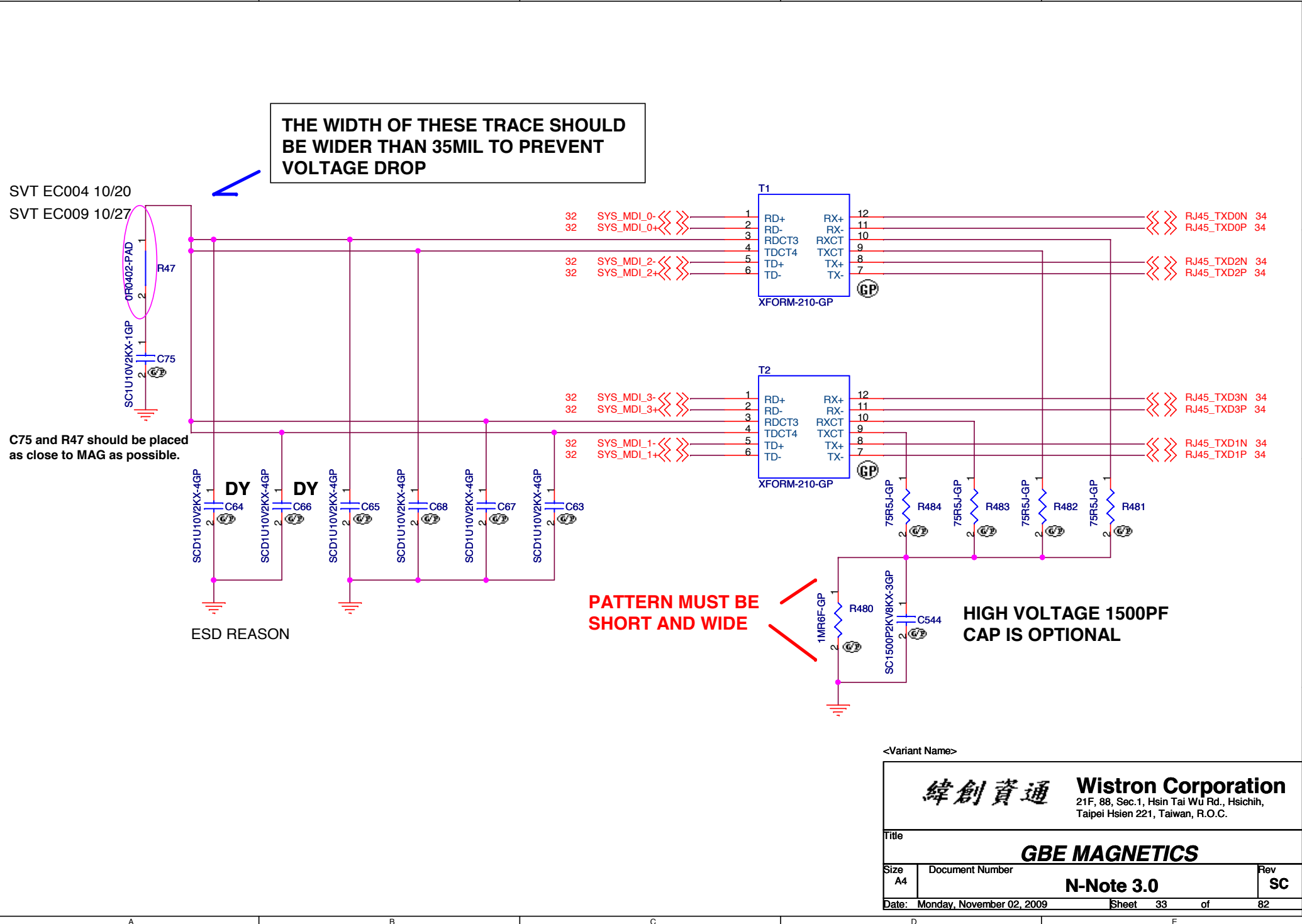


<Variant Name>


		Vendor P/N	Wistron P/N	B/S P/N
1st	Pericom	PI3L500AZFEX	73.3L500.003	41R0539AA
2nd	TI	TS3L500AERHUR	73.3L500.A0V	41R0539BA

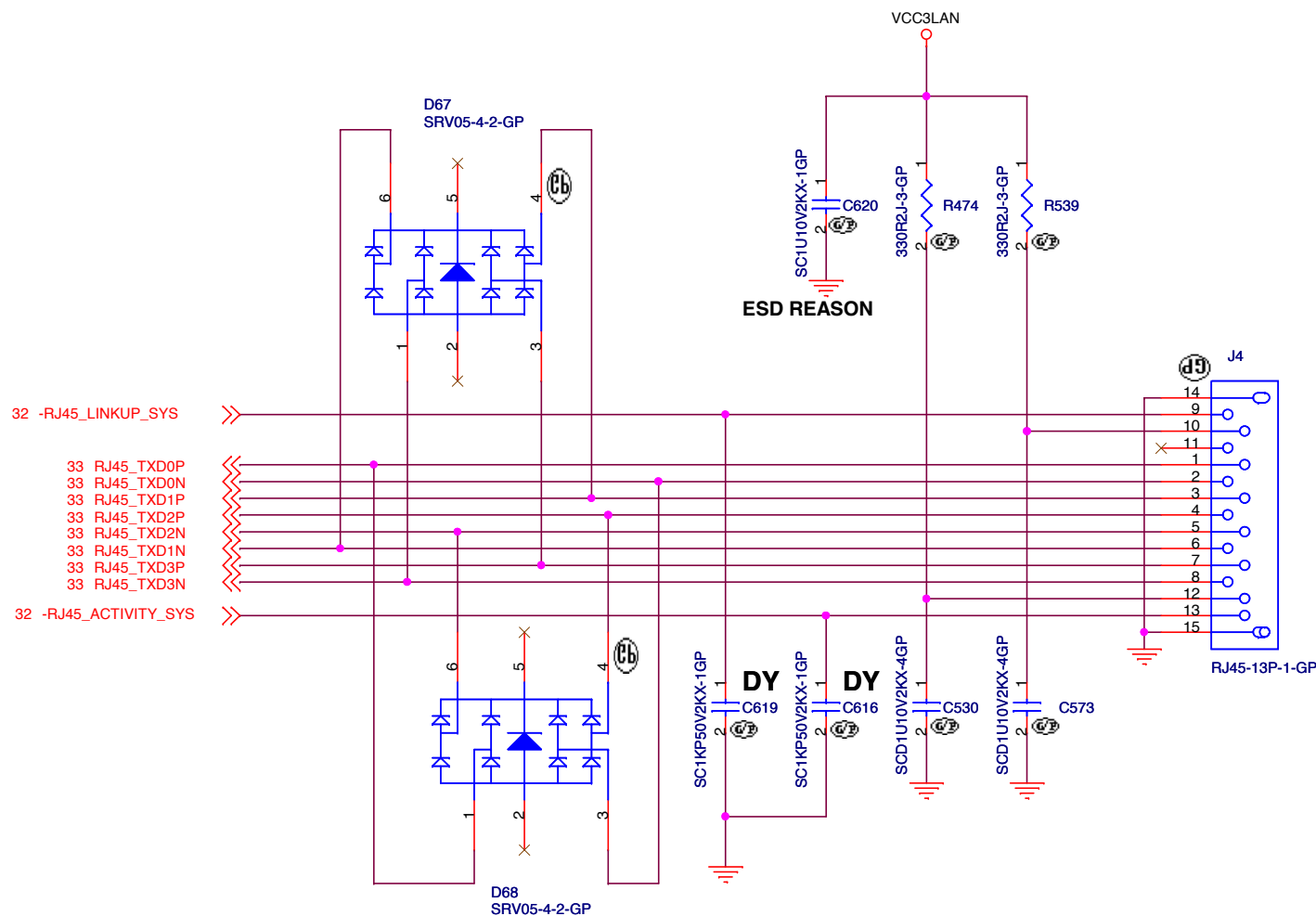
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		GBE LAN SW	
Size A4	Document Number	N-Note 3.0	
Date: Monday, November 02, 2009	Sheet 32 of 82	Rev	SC

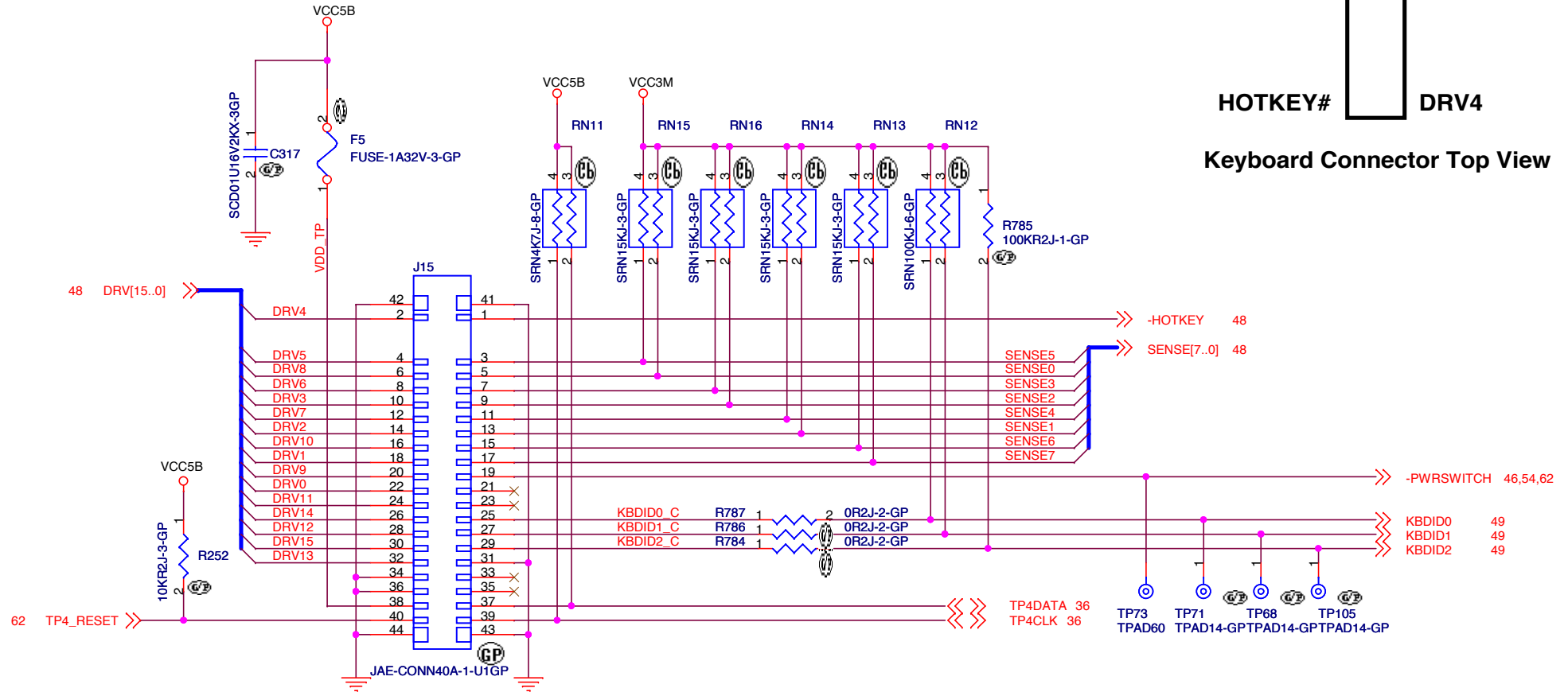


<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GBE MAGNETICS			
Size A4	Document Number N-Note 3.0		Rev SC
Date:	Monday, November 02, 2009	Sheet 33 of	82



Keyboard Connector



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

KEYBOARD CONN

Size

A4

Document Number

N-Note 3.0

Rev

SC

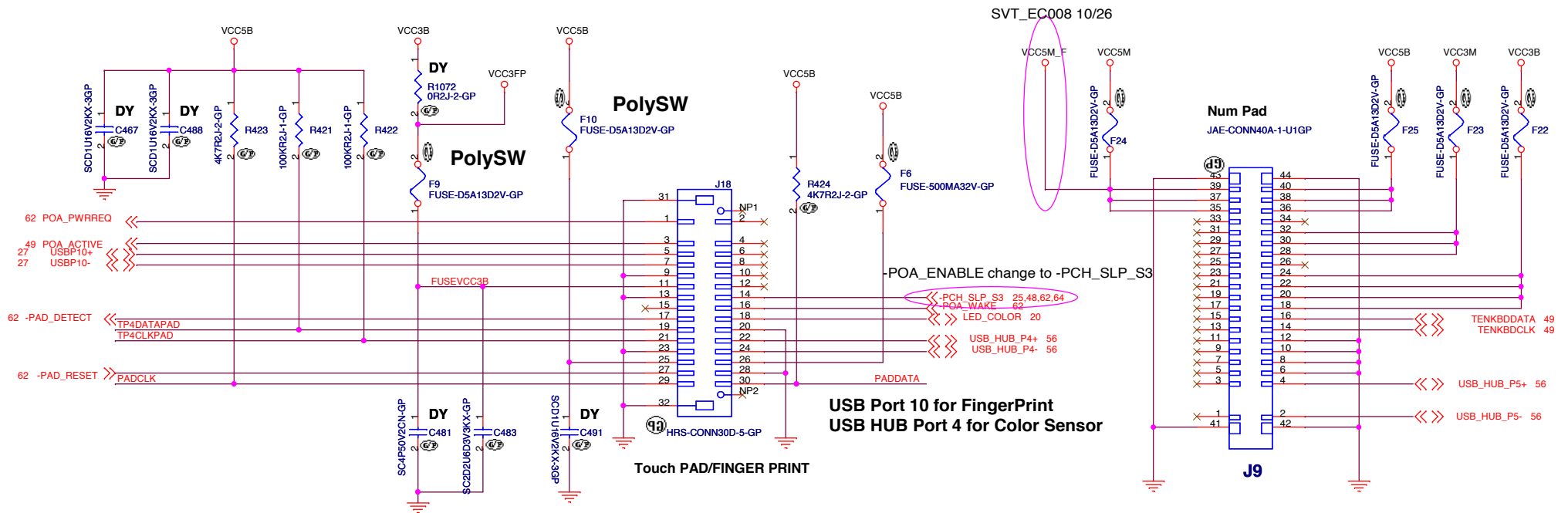
Date: Monday, November 02, 2009

Sheet

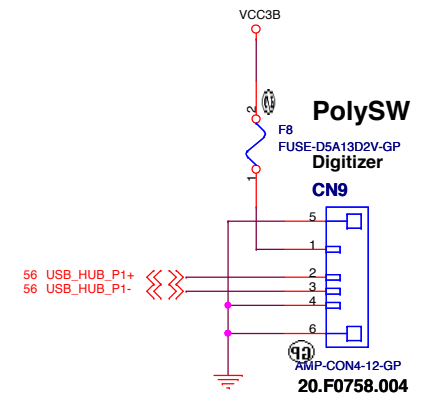
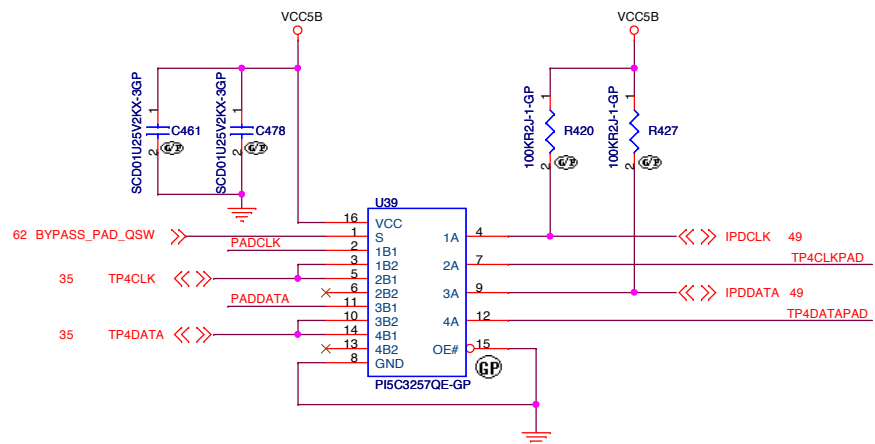
35

of

82

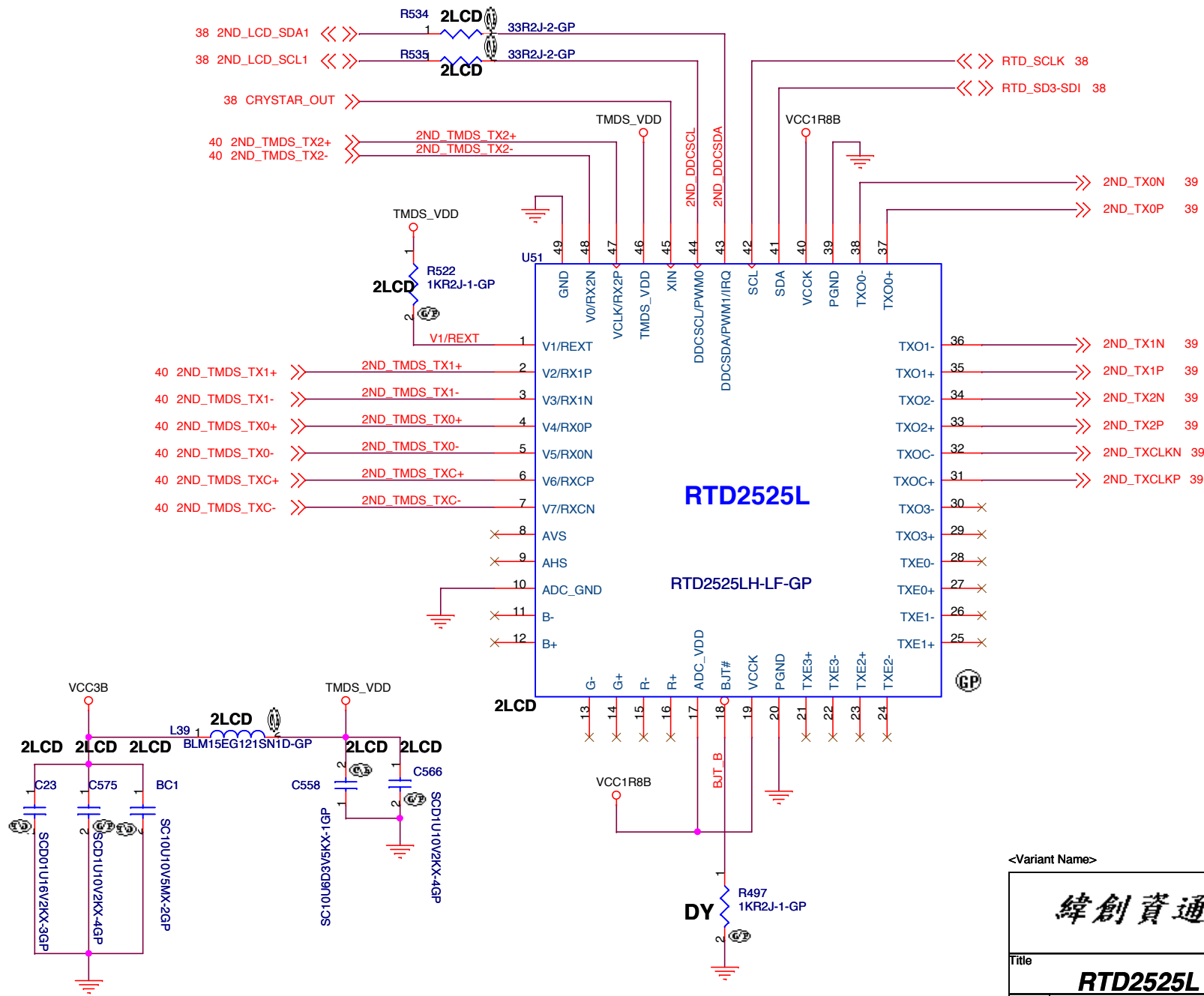


USE FSTU3257(FAIRCHILD) OR PI5C3257C(PERICOM)



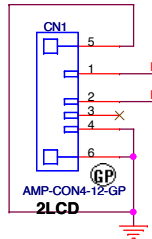
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
TOUCH PAD CONNECTOR	
Title Size Custom	Document Number N-Note 3.0
Date: Monday, November 02, 2009	Sheet 36 of 82
Rev SC	

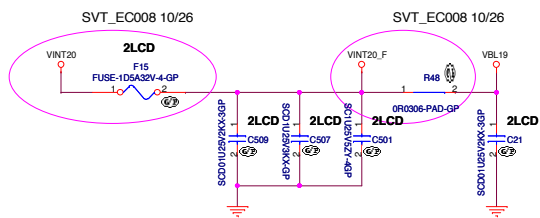
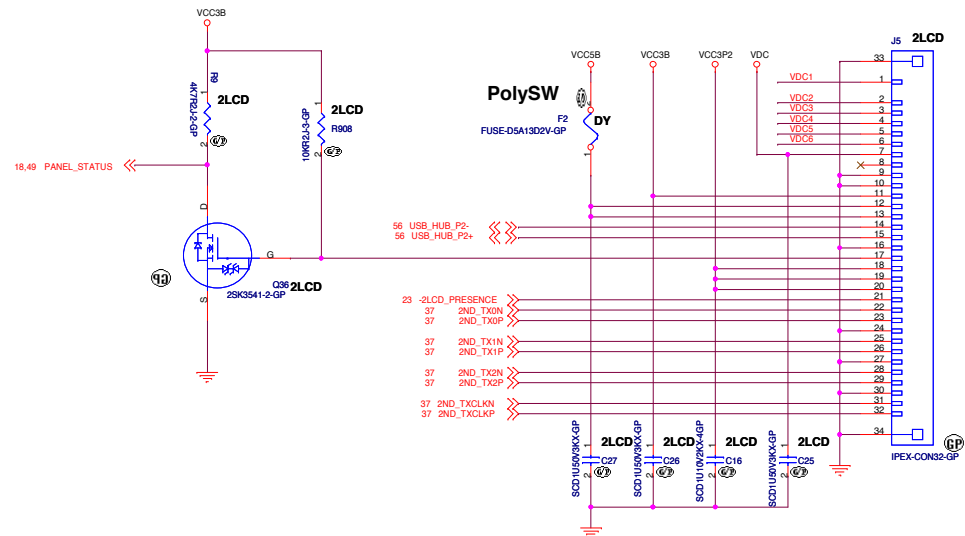
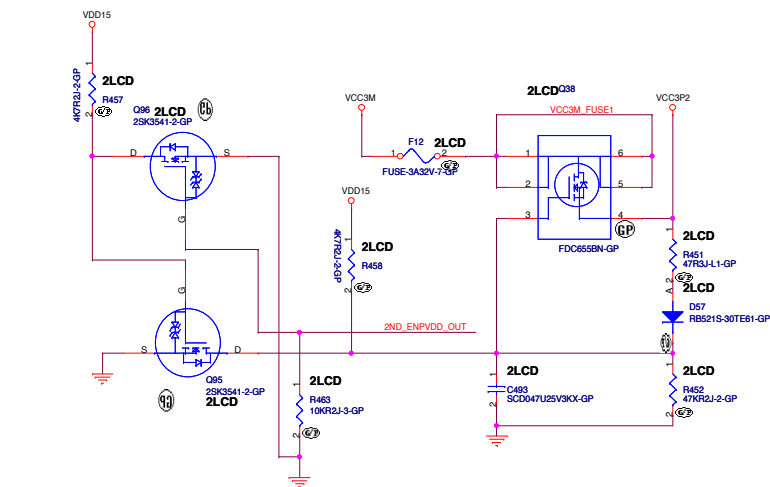


<Variant Name>

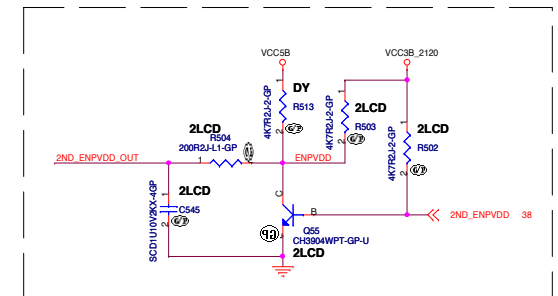
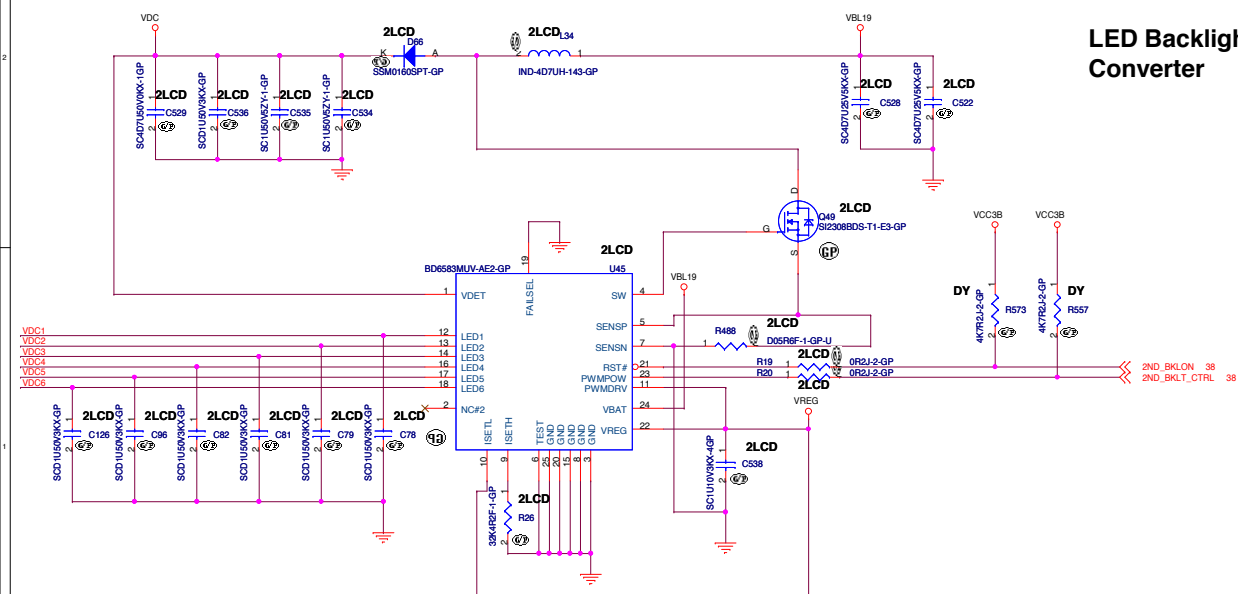
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RTD2525L (1/2)			
Size A4	Document Number N-Note 3.0		Rev SC
Date:	Monday, November 02, 2009	Sheet 37 of	82



	2nd LCD Non 2nd LCD Common planar	NON 2nd LCD Planar
U44	Yes	No
RN5	No	Yes



LED Backlight Converter



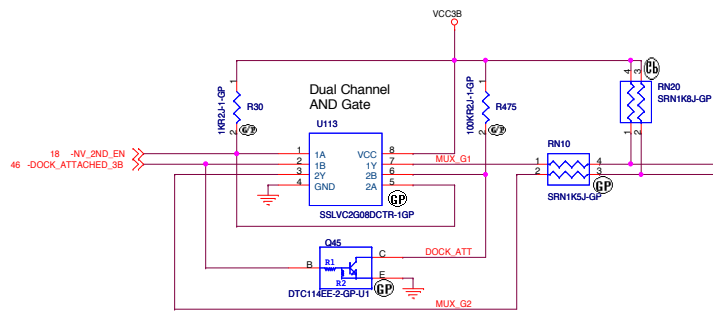
2008-10-22 Realtek FAE suggestion us to improve for 2'nd LCD flashing issue

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

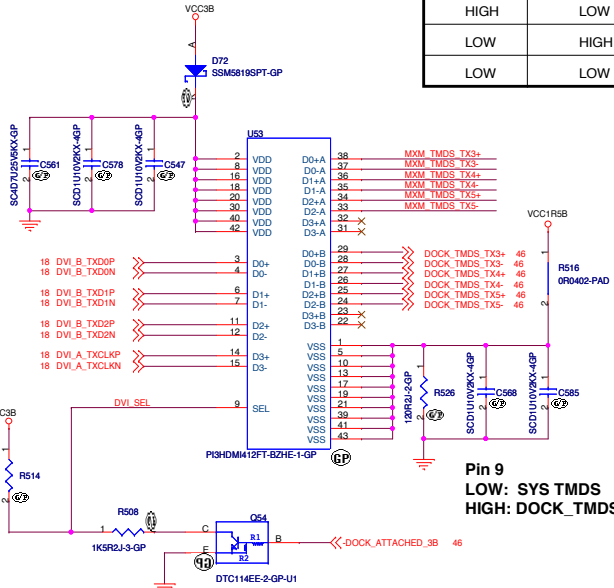
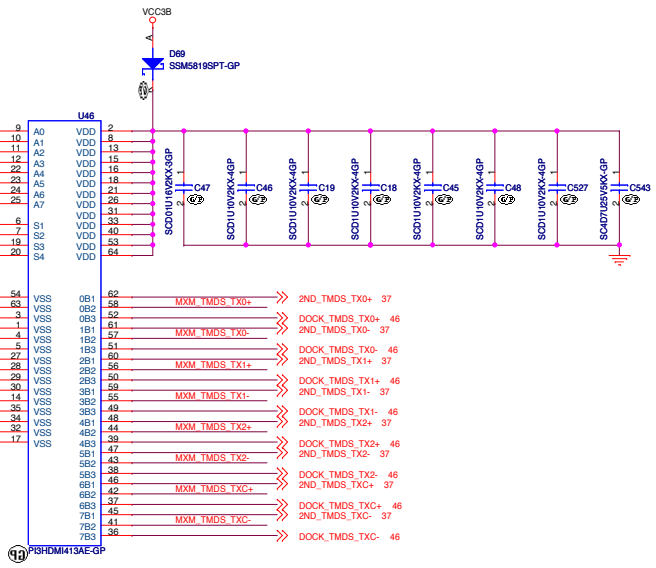
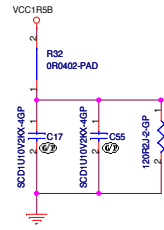
2'ND LCD CONNECTOR

Size Custom Document Number N-Note 3.0 Rev SC

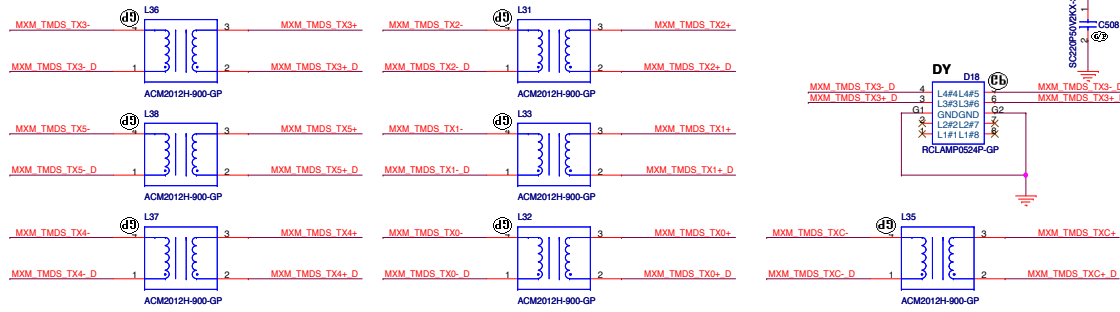
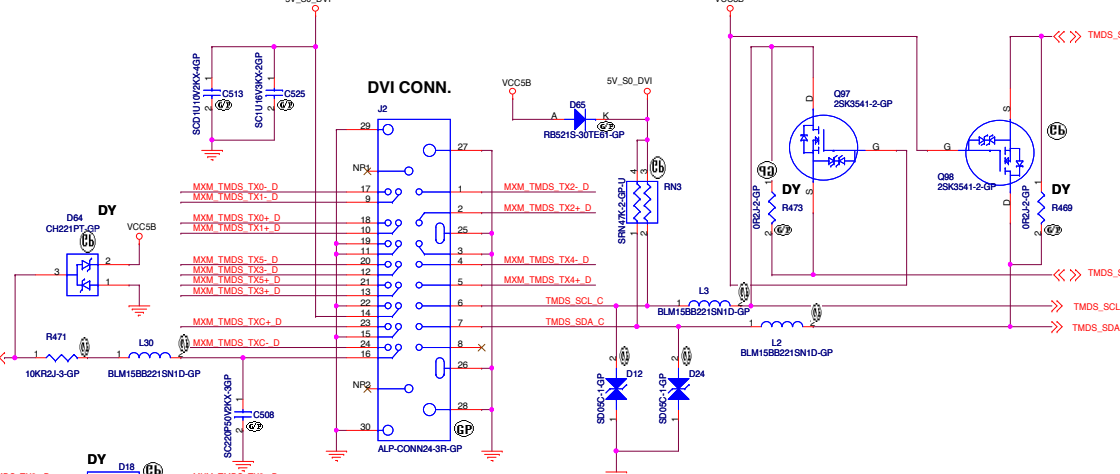
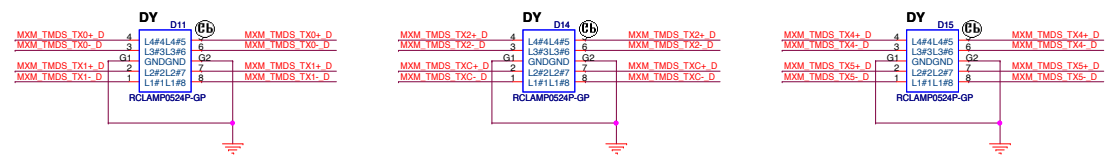
Date: Monday, November 02, 2009 Sheet 39 of 62



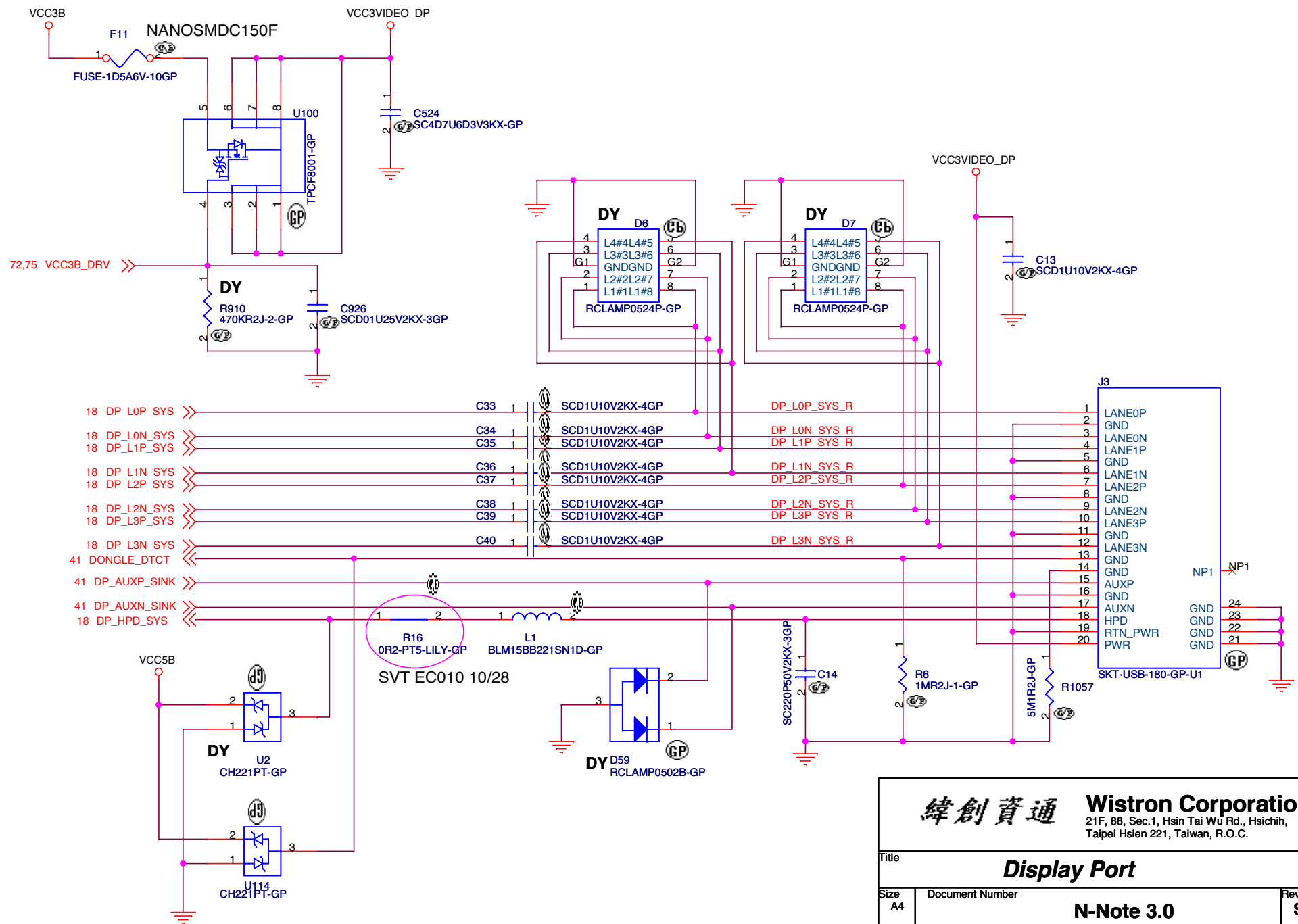
INPUTS		OUTPUTS		RESULT
-NV_2ND_EN	-DOCK_ATTACHED_3B	S1	S2	
HIGH	HIGH	HIGH	LOW	SYS DVI
HIGH	LOW	LOW	HIGH	DOCK DVI
LOW	HIGH	LOW	LOW	2ND DISPLAY
LOW	LOW	LOW	LOW	



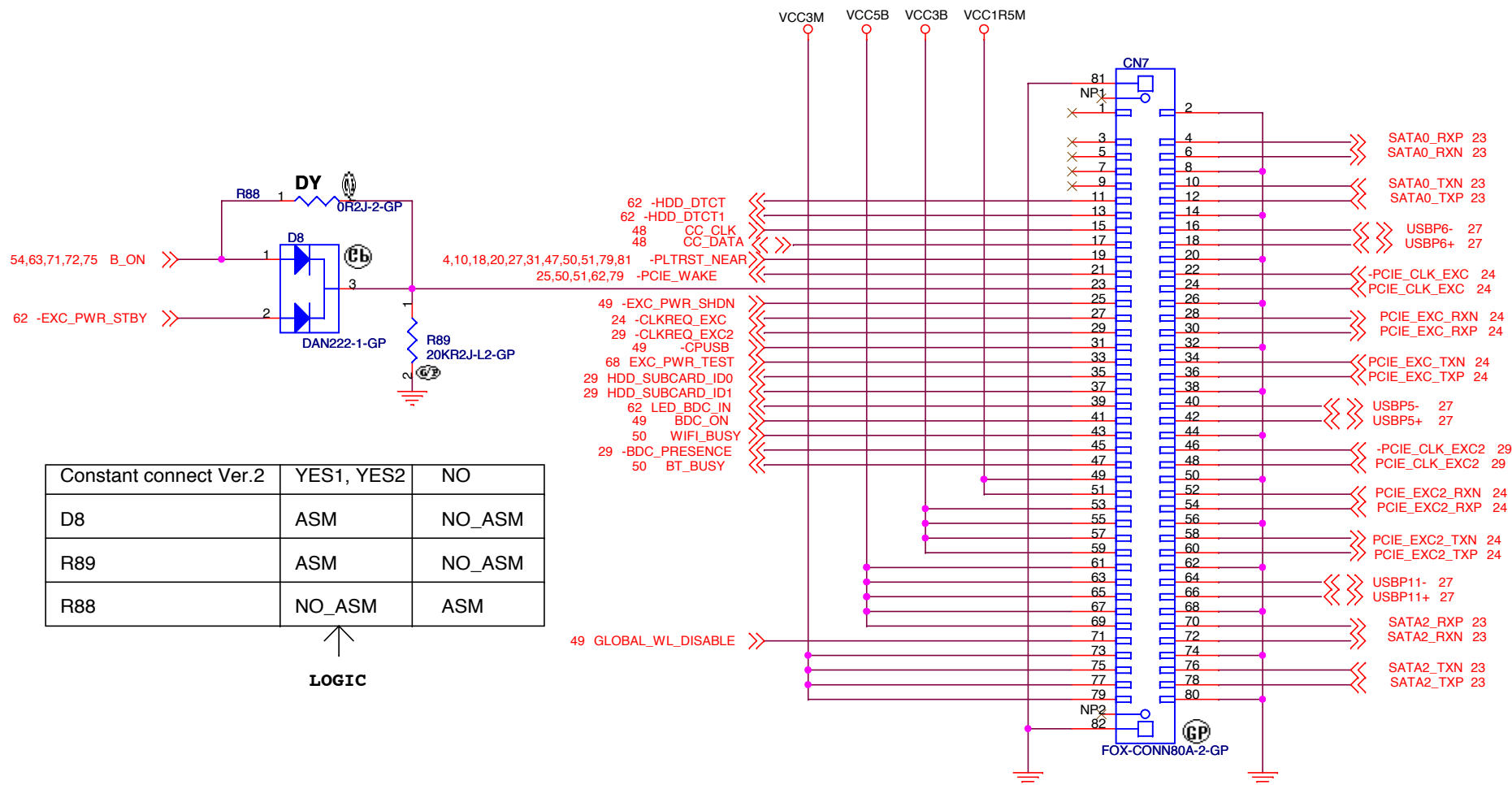
Pin 9
LOW: SYS TMDS
HIGH: DOCK TMDS







HDD IO SUB CARD Connector



Constant connect Ver.2	YES1, YES2	NO
D8	ASM	NO_ASM
R89	ASM	NO_ASM
R88	NO_ASM	ASM

LOGIC

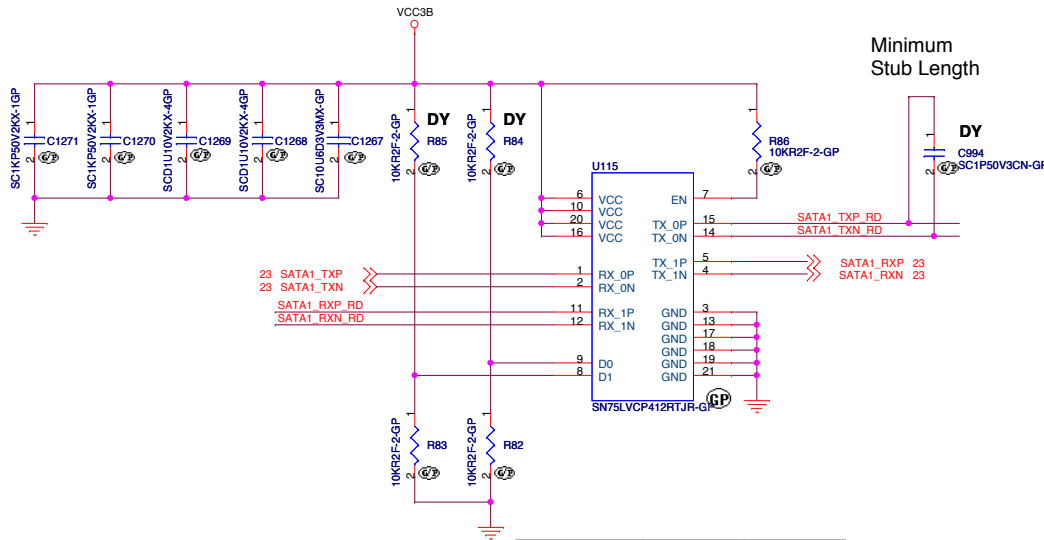
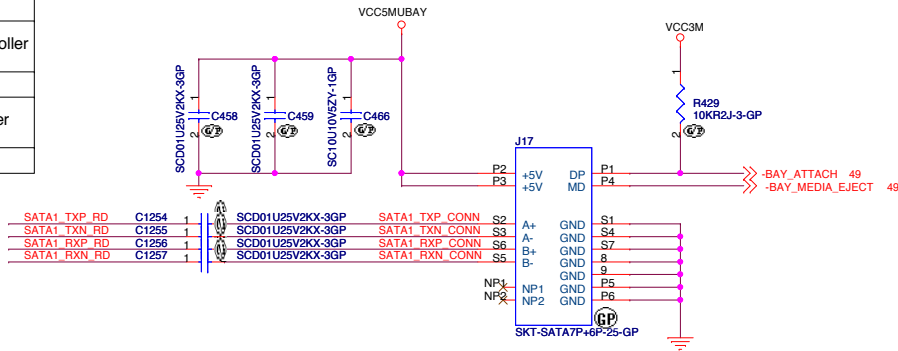
<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title SATA HDD CONN			
Size A4	Document Number N-Note 3.0		Rev SC
Date: Monday, November 02, 2009		Sheet 43	of 82

SATA ODD/BAY Connector

SATA SIGNAL SEGMENT		
S1	GND	Differential signal pair from host controller
S2	A+	
S3	A-	
S4	GND	Differential signal pair to host controller
S5	B-	
S6	B+	
S7	GND	

SATA POWER SEGMENT		
P1	DP	Device Present
P2	+5V	
P3	+5V	
P4	MD	Manufacturing Diagnostic
P5	GND	
P6	GND	

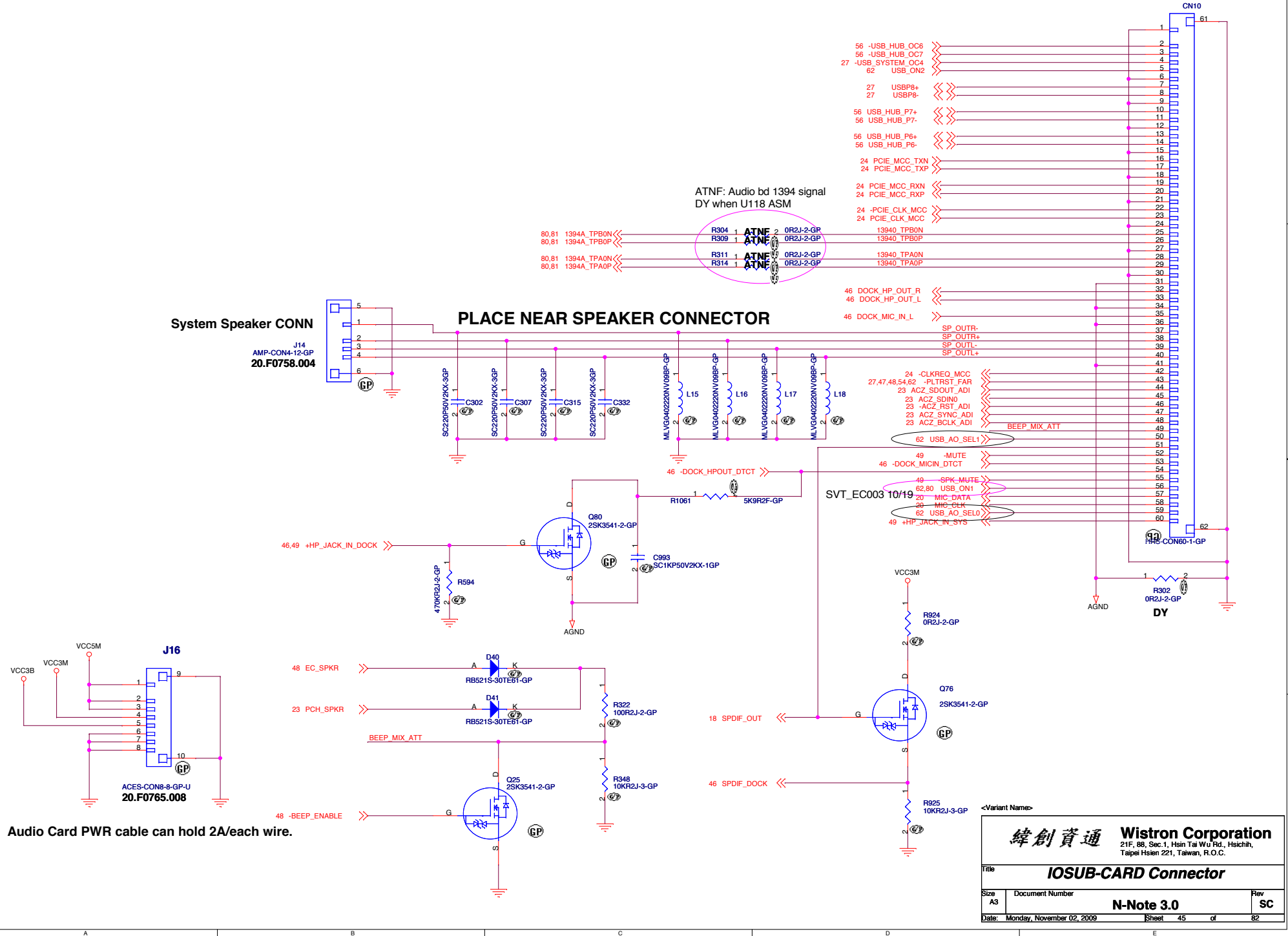


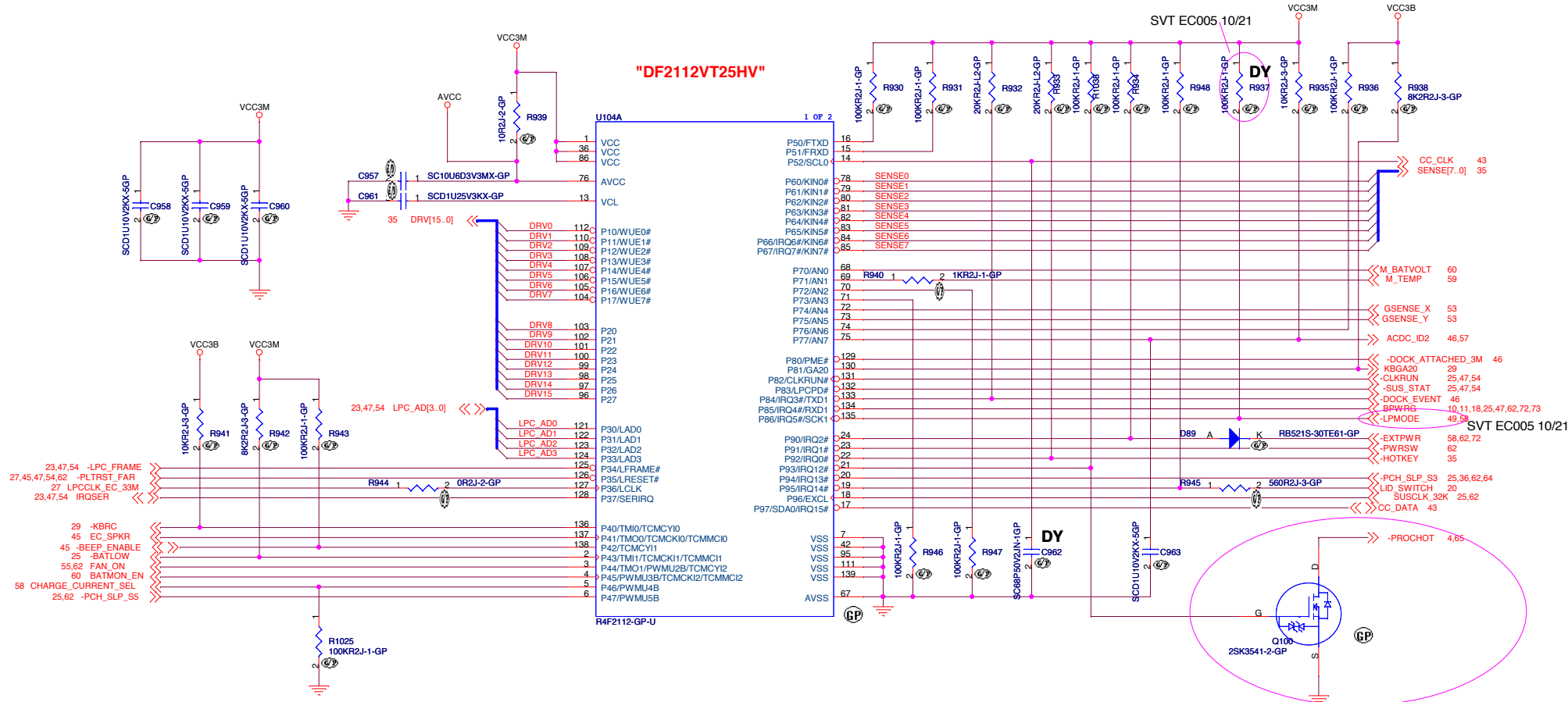
EN	D0	D1	CH-0	CH-1
0	X	X	STANDBY	STANDBY
1	0	0	Standard	Standard
1	1	0	BOOST	Standard
1	0	1	Standard	BOOST
1	1	1	BOOST	BOOST

LOGIC

<Variant Name>

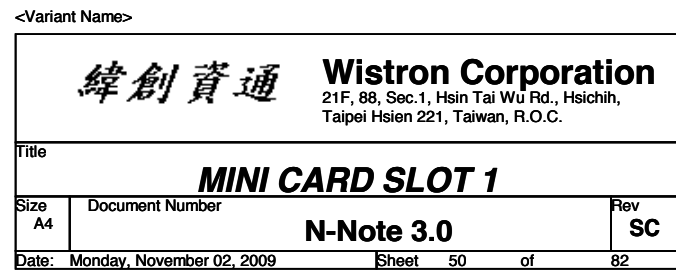
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SATA BAY I/F CONN			
Size	Document Number		Rev
N-Note 3.0			SC
Date:	Monday, November 02, 2009	Sheet 44 of	82





[illegible]

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www.vinafix.vn

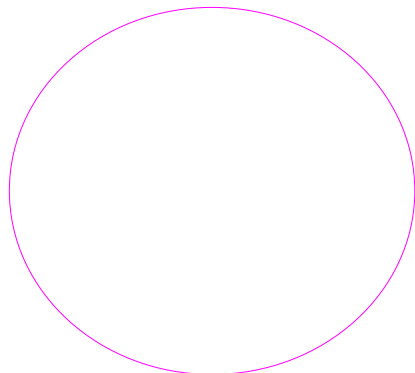
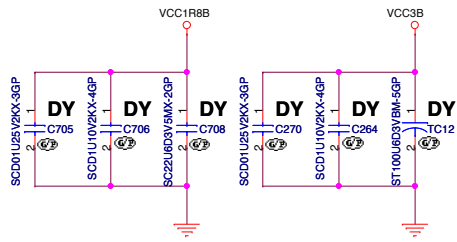


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

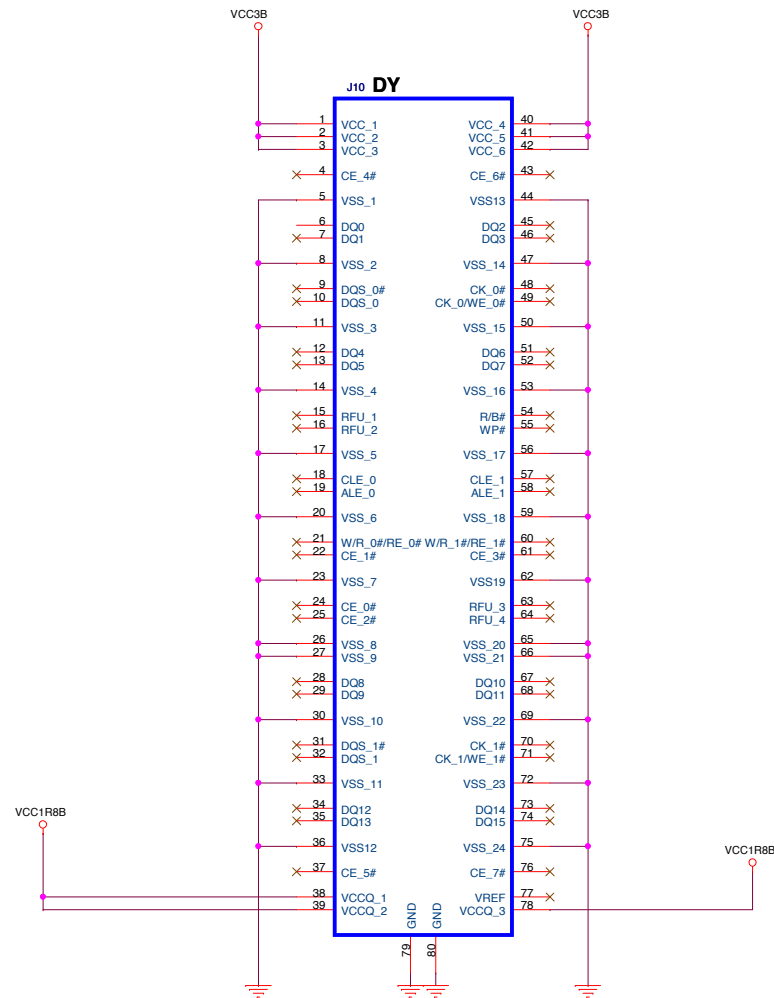
MINI CARD SLOT 2

N-Note 3.0

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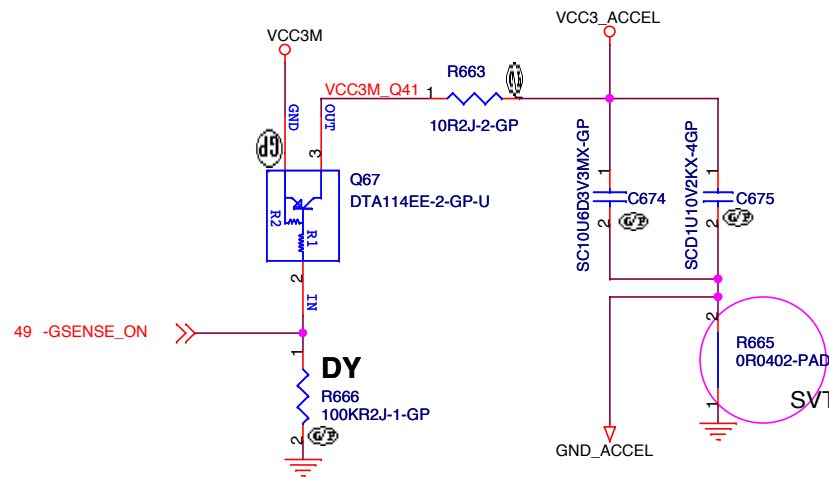
SVT_EC004 10/20



J10 P/N should be 62.10034.361

<Variant Name>

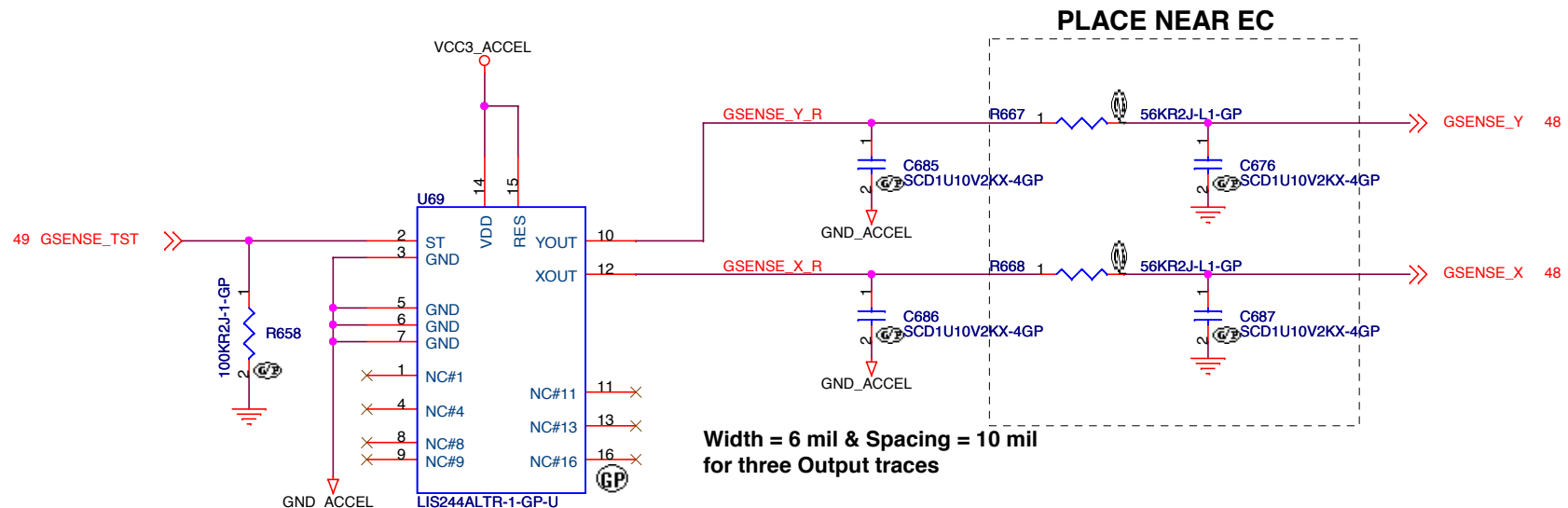
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
TURBO MEMORY SLOT			
Title Size A3	Document Number N-Note 3.0	Rev SC	
Date: Monday, November 02, 2009		Sheet 52 of 82	



Layout Comment :

- (1) Place Q67, R666, R663, C674, C675, R665, C685 and C686 close to U69.
- (2) Avoid routing under DCDC switching area.

SVT_EC009 10/27



PLACE NEAR EC

Width = 6 mil & Spacing = 10 mil
for three Output traces

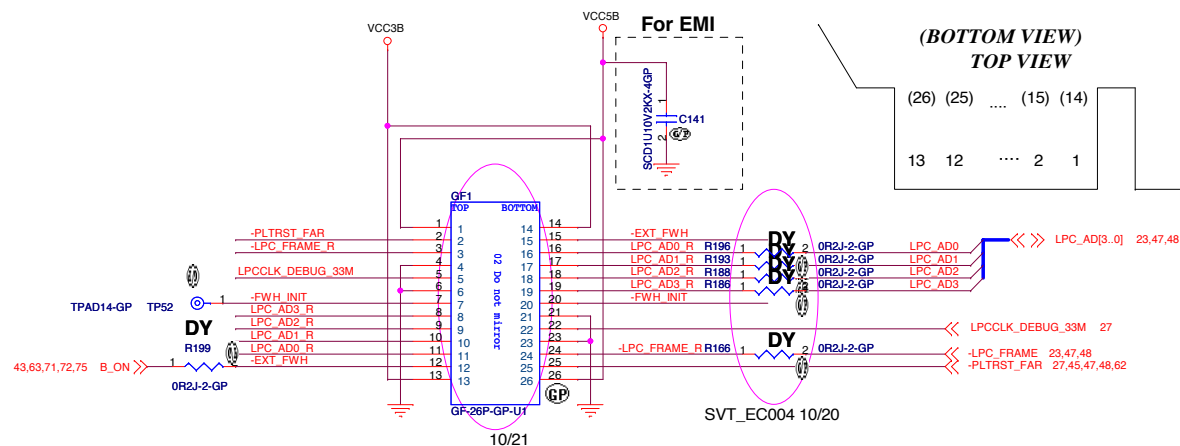
[Source Candidate]

STMicro LIS244AL 41R0525AA
STMicro LIS34AL 41R0828AA

<Variant Name>

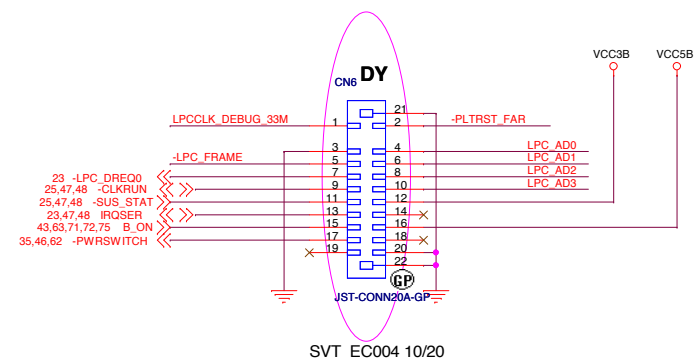
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size A4		Document Number G-SENSOR	
Date: Monday, November 02, 2009		Rev SC	
Sheet 53 of 82		N-Note 3.0	

Golden Finger for Debug Board



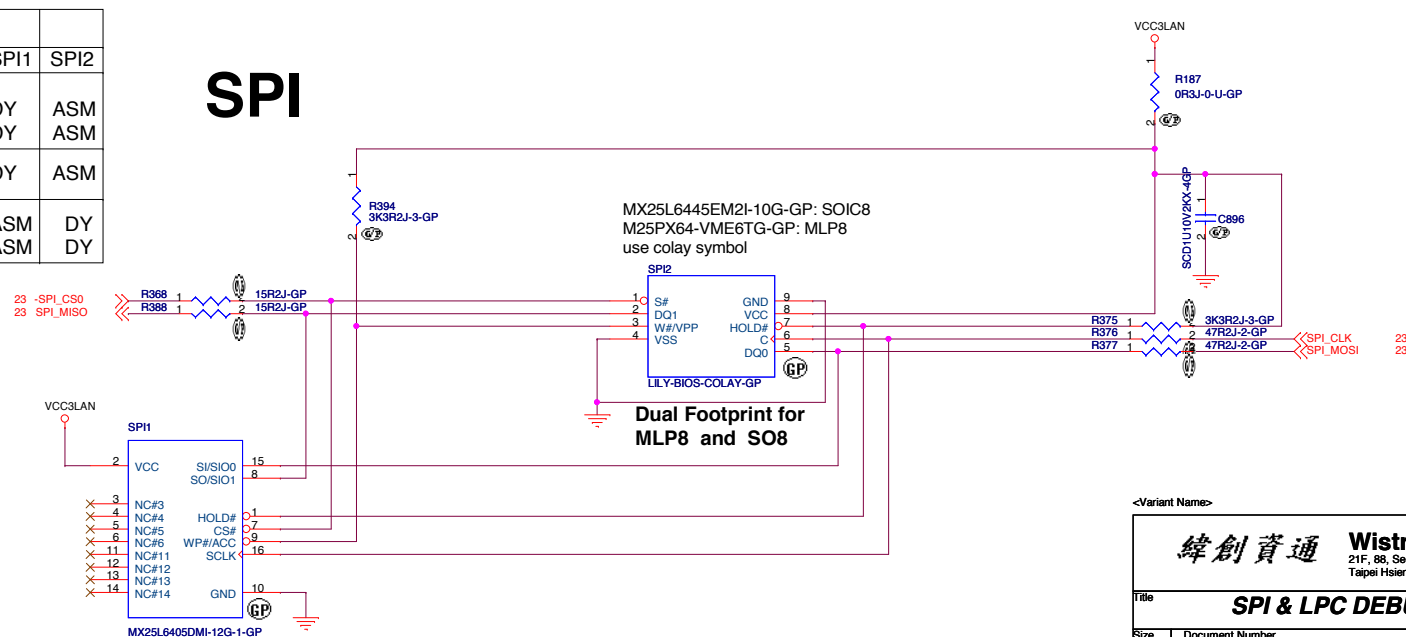
Ref Des	Enable	Disable
CN6	ASM	NO_ASM
R814	ASM	NO_ASM
R196	ASM	NO_ASM
R193	ASM	NO_ASM
R188	ASM	NO_ASM
R186	ASM	NO_ASM
R166	ASM	NO_ASM

SVT_EC004 10/20



64M-bit SPI Flash				
			SPI1	SPI2
SO8	MACRONIX WINBOND	MX25L6445EM21-10G MX25X64BVSSIG	DY DY	ASM ASM
MLP8	NUMONYX	M25PX64-VME6TG	DY	ASM
SO16	MACRONIX WINBOND	MX25L6405DMI-12G MX25X64VSFIG	ASM ASM	DY DY

SPI



<Variant Name>

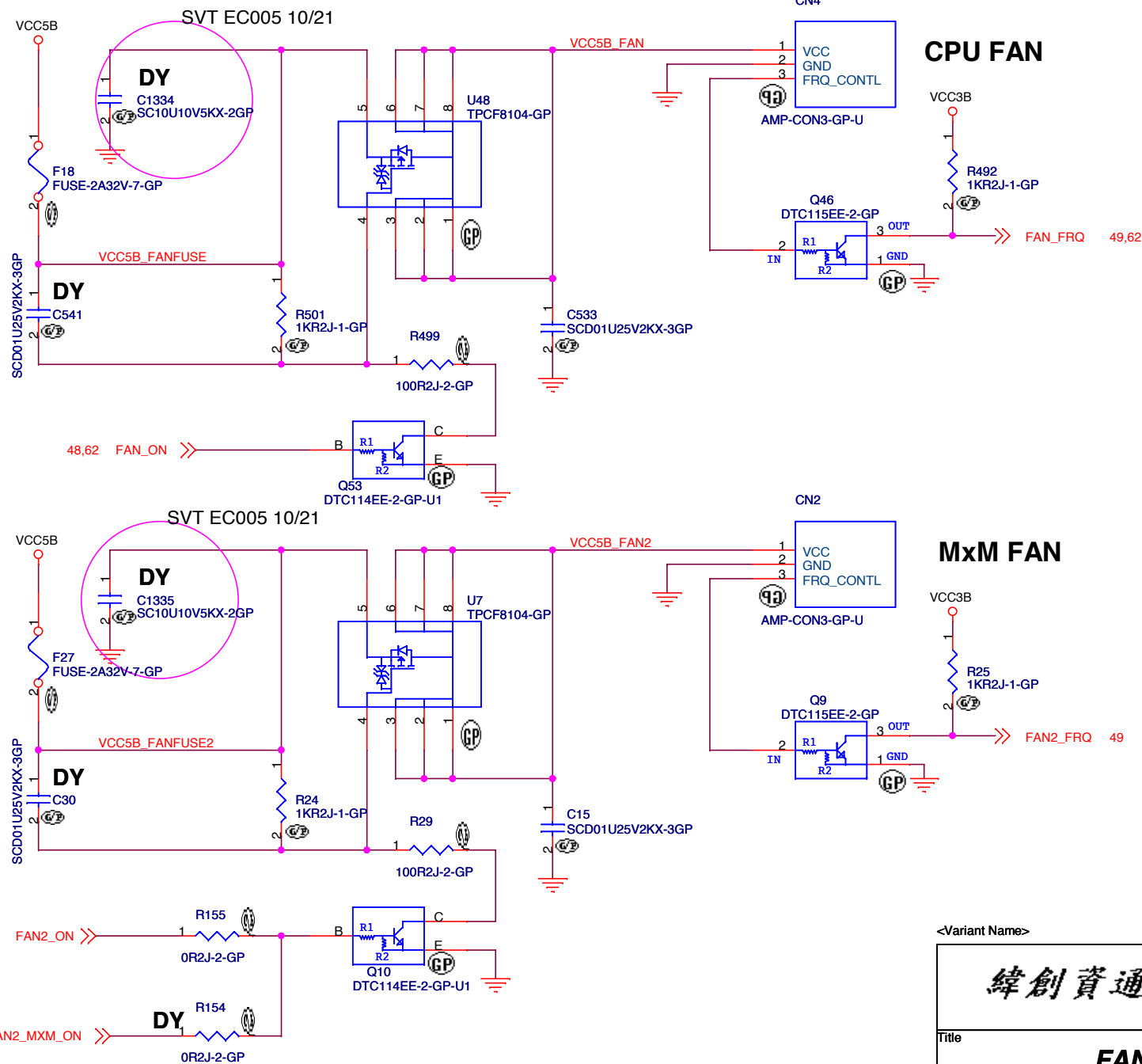
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **SPI & LPC DEBUG CARD**

Size A3	Document Number N-Note 3.0	Rev SC
------------	--------------------------------------	------------------

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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

FAN CONTROL

Size
A4

Document Number

N-Note 3.0

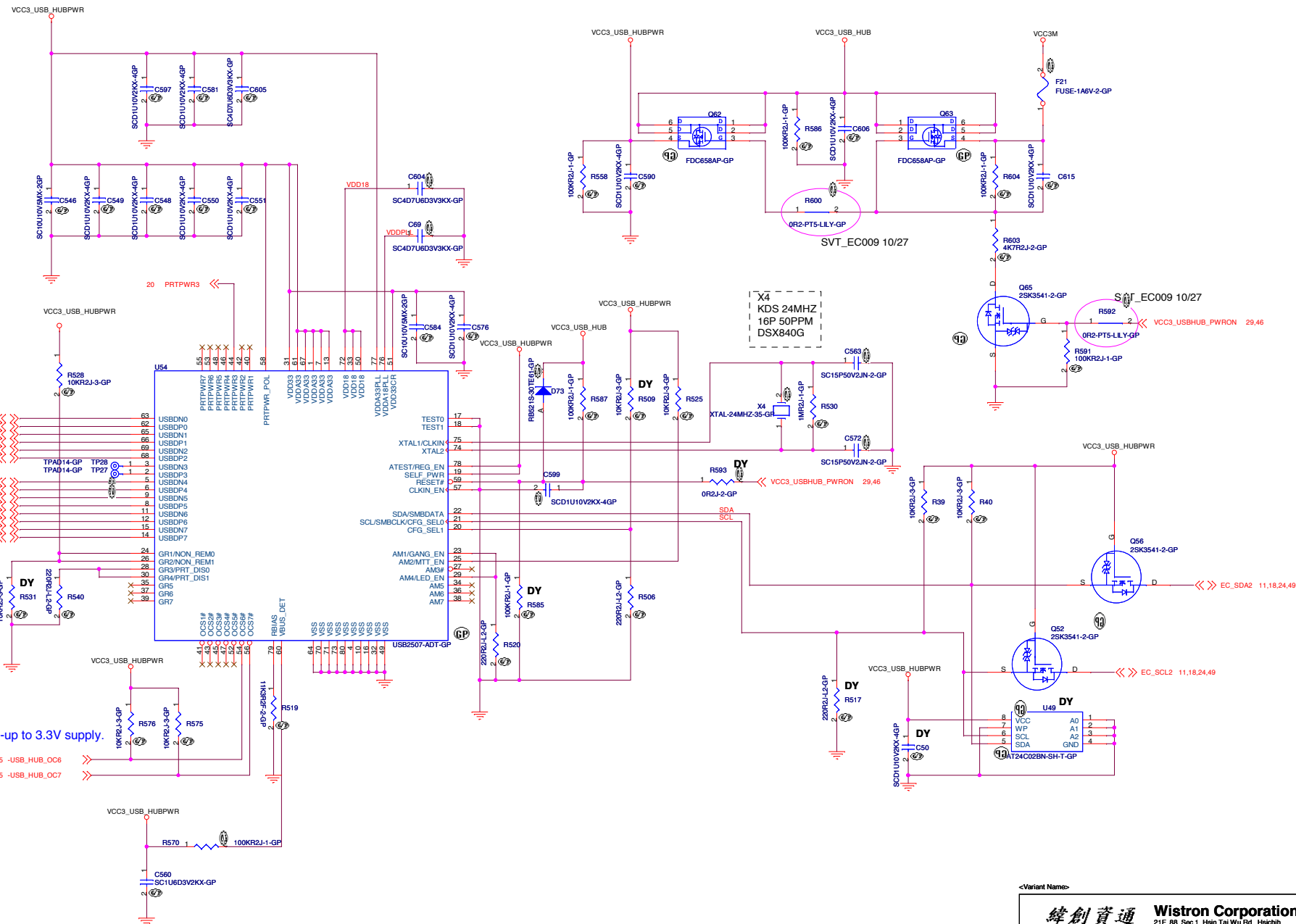
Rev
SC

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Port 0 : From PCH
 Port 1 : Digitizer
 Port 2 : 2nd LCD
 Port 3 : Reserved
 Port 4 : Color Sensor
 Port 5 : Num Pad
 Port 6 : System Port 3
 Port 7 : System Port 4

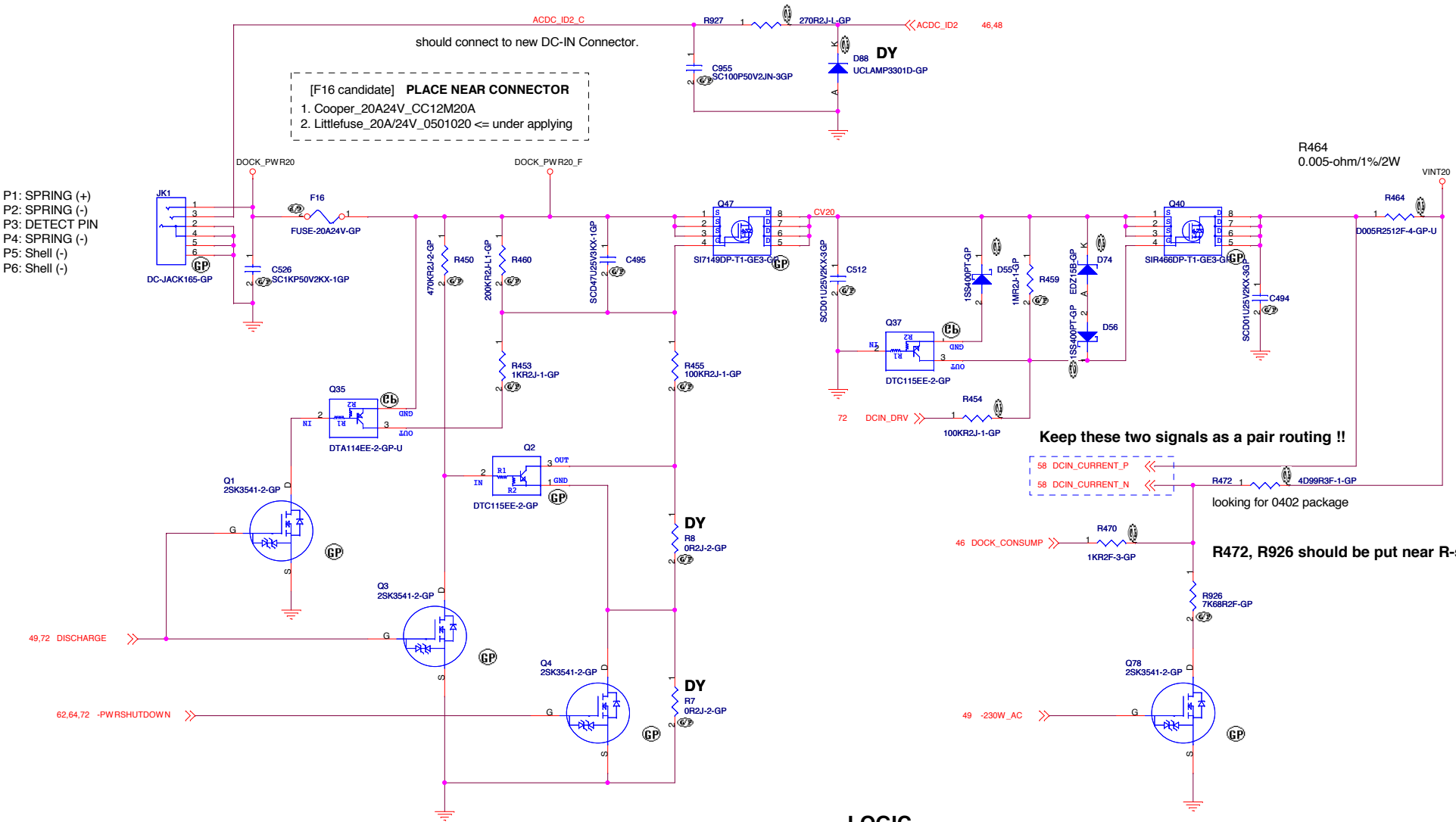
OCSx# has internal pull-up to 3.3V supply.



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
USB HUB(USB2507-ADT)			
Size	Document Number	Rev	
Custom		SC	
N-Note 3.0			
Date:	Monday, November 02, 2009	Sheet	56 of 82

P1: SPRING (+)
P2: SPRING (-)
P3: DETECT PIN
P4: SPRING (-)
P5: Shell (-)
P6: Shell (-)

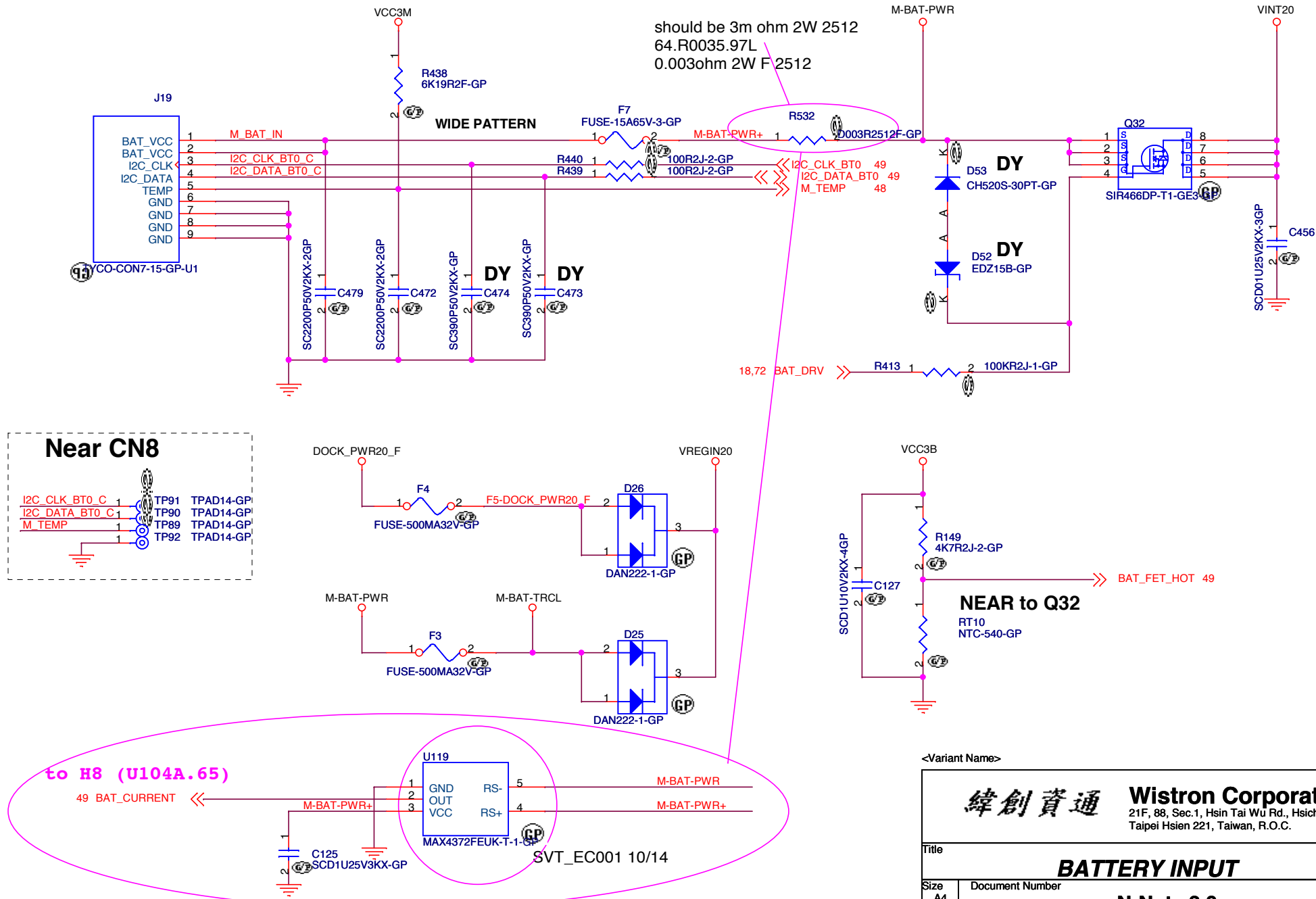


LOGIC
↓

PEAK SHIFT	YES	NO
R8	NO-ASM	ASM
R7	ASM	NO-ASM
Q2	ASM	NO-ASM
Q3	ASM	NO-ASM

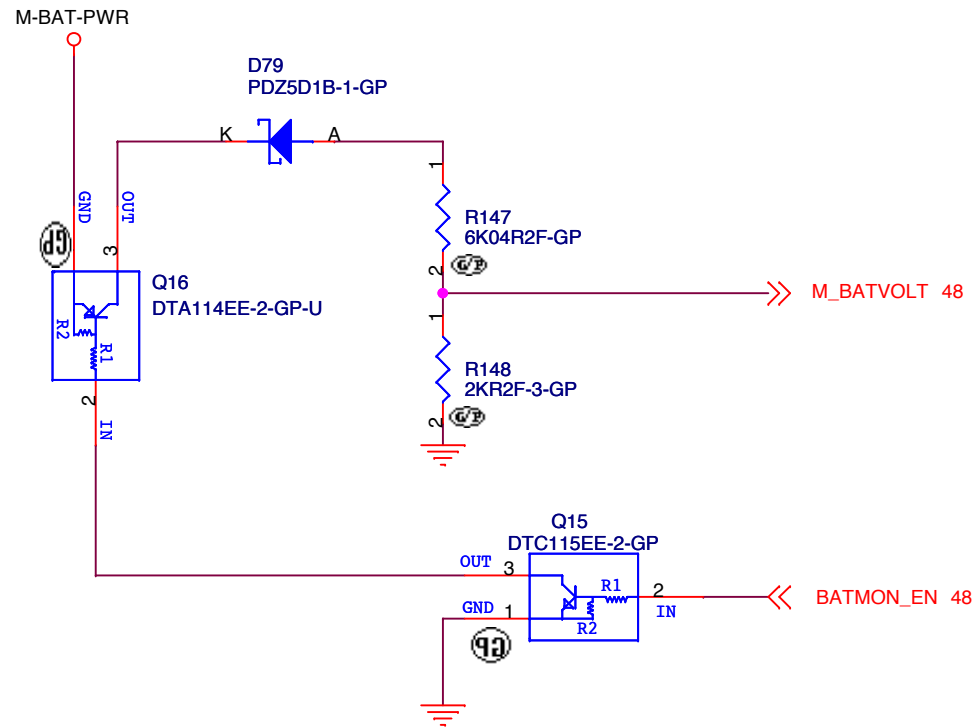
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DC-IN AND CHARGER (1/2)		
Size A3	Document Number N-Note 3.0	Rev SC
Date: Monday, November 02, 2009	Sheet 57 of 82	



<Variant Name>	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
BATTERY INPUT	
Size A4	Document Number
N-Note 3.0	
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$$V_{OUT} = 0.249 (V_{BAT} - 5)$$



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BATTERY MONITOR

Size
Custom

Document Number

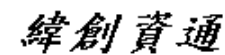
N-Note 3.0

Rev
SC

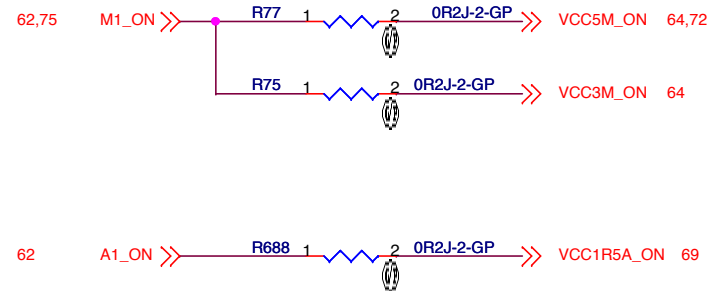
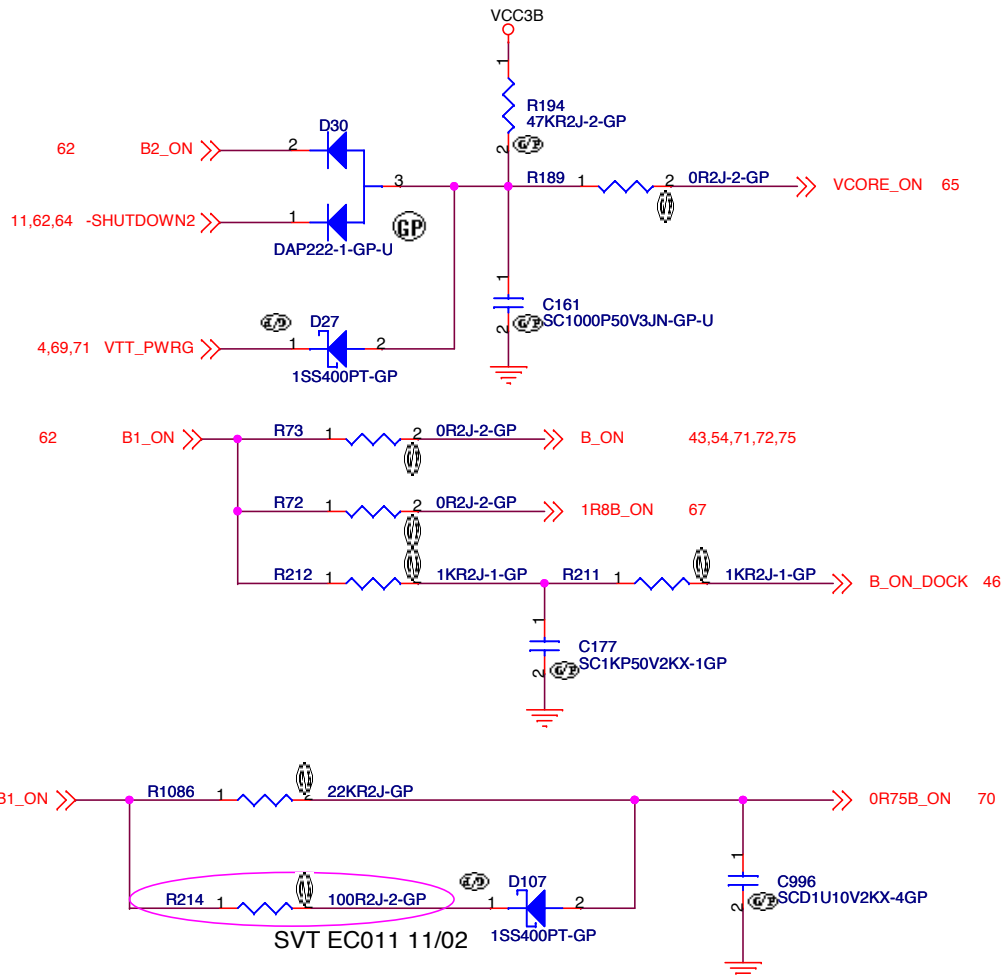
Date: Monday, November 02, 2009

Sheet 60 of

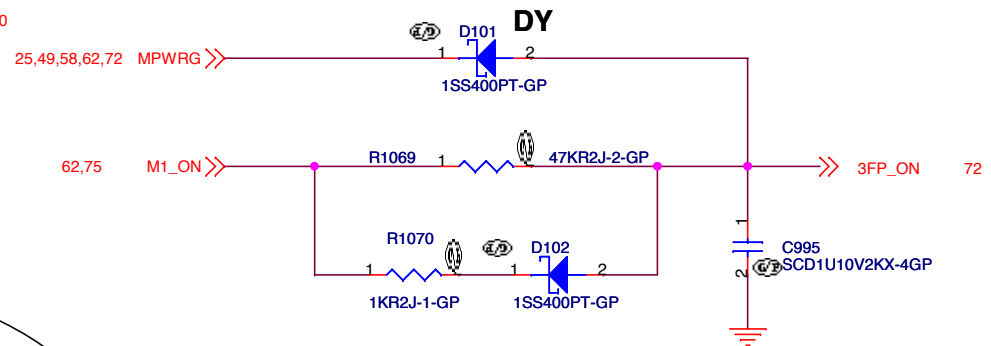
82



Title			
CHARGER SELECT			
Size A4	Document Number N-Note 3.0		Rev SC
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Remove Power Sequence backup for SLP_LAN#



Remove Power Sequence backup for SLP_M#

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

POWER SEQUENCE

Size
A4

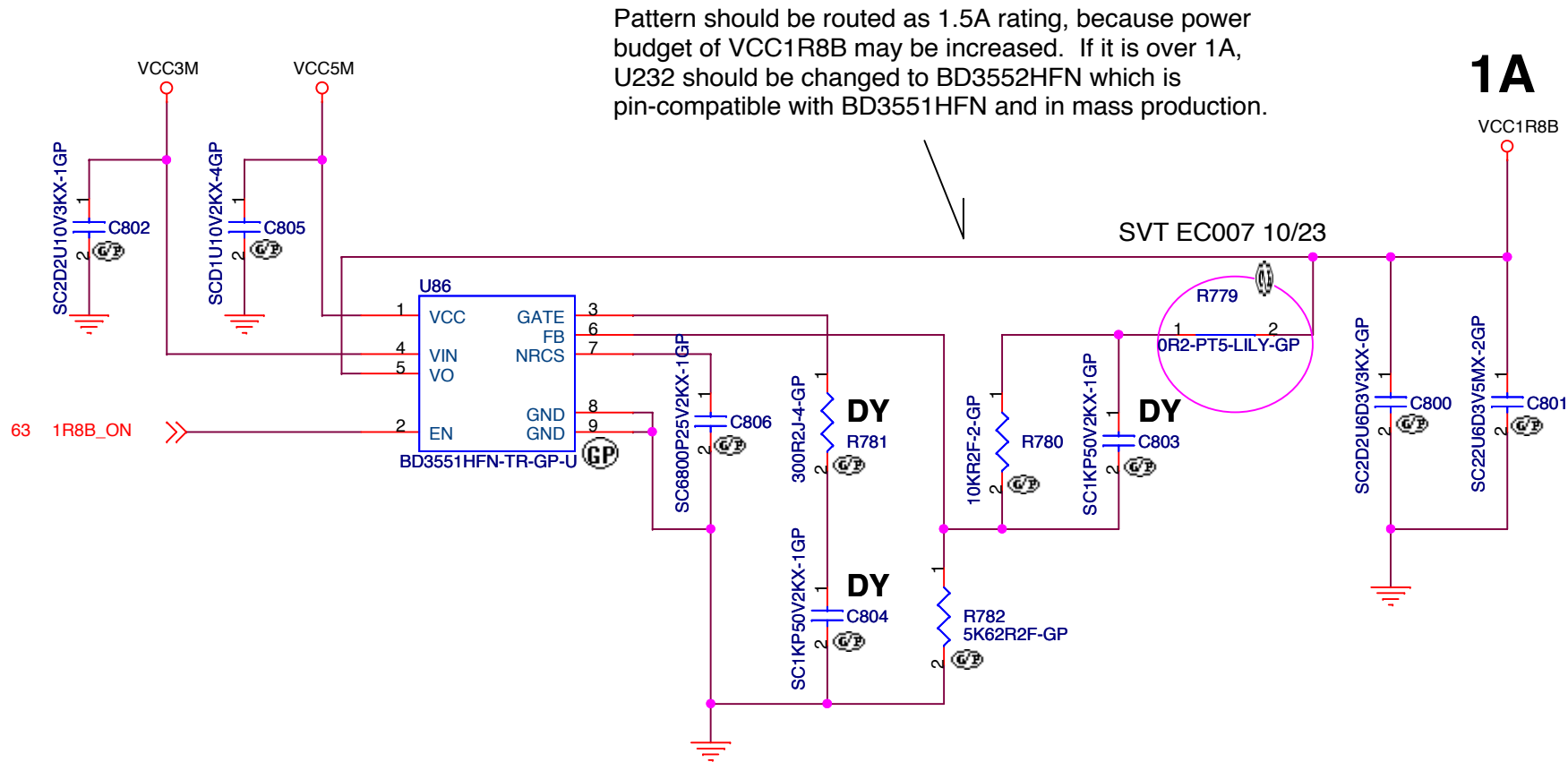
Document Number

N-Note 3.0

Rev
SC

Date: Tuesday, November 03, 2009

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DC-DC VCC1R8B

Size
A

Document Number

N-Note 3.0

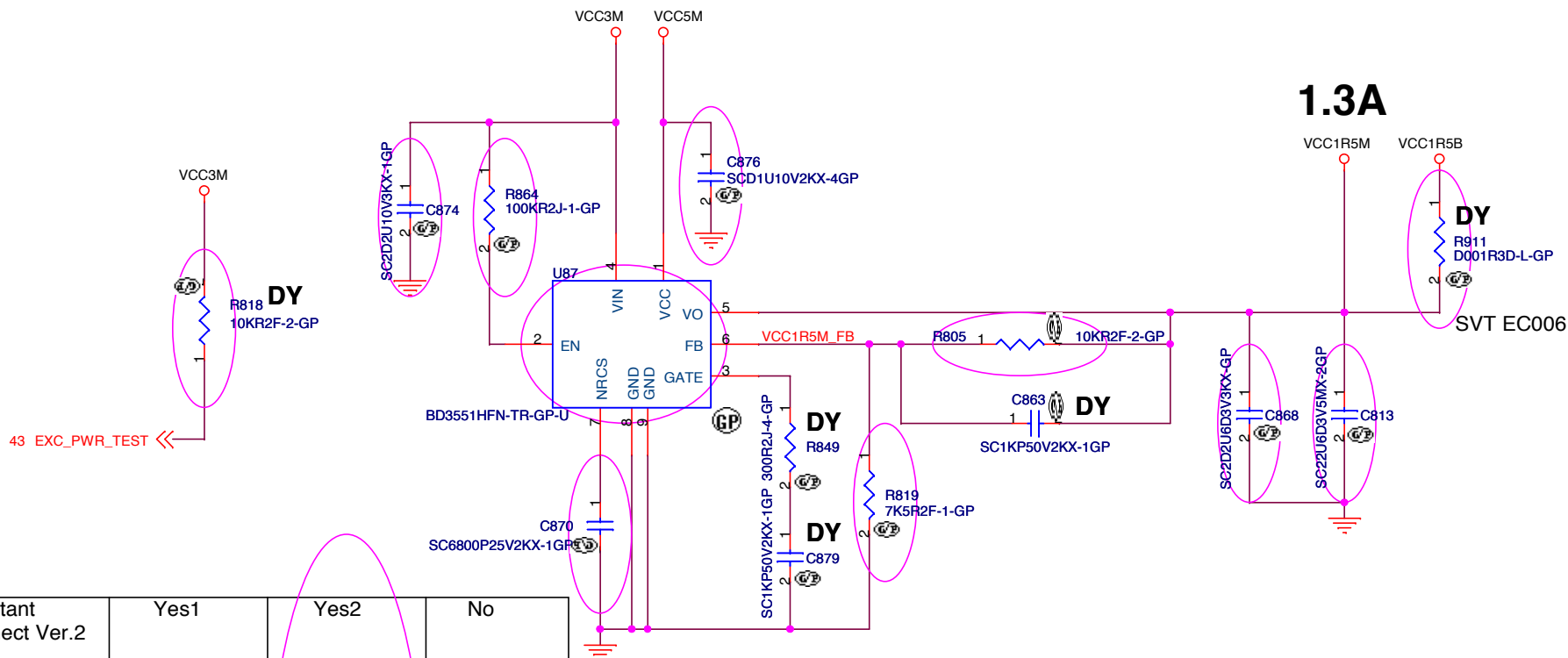
Rev
SC

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Constant Connect Ver.2	Yes1	Yes2	No
R818 R911	ASM ASM	NO ASM NO ASM	NO ASM ASM
U87	NO ASM	ASM	NO ASM
R864	NO ASM	ASM	NO ASM
C874	NO ASM	ASM	NO ASM
C876	NO ASM	ASM	NO ASM
C870	NO ASM	ASM	NO ASM
R849	NO ASM	NO ASM	NO ASM
C879	NO ASM	NO ASM	NO ASM
R805	NO ASM	ASM	NO ASM
R819	NO ASM	ASM	NO ASM
C863	NO ASM	NO ASM	NO ASM
C868	NO ASM	ASM	NO ASM
C813	NO ASM	ASM	NO ASM

Logic

SVT EC010 10/28

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VCC1R5M

Size
A4

Document Number

N-Note 3.0

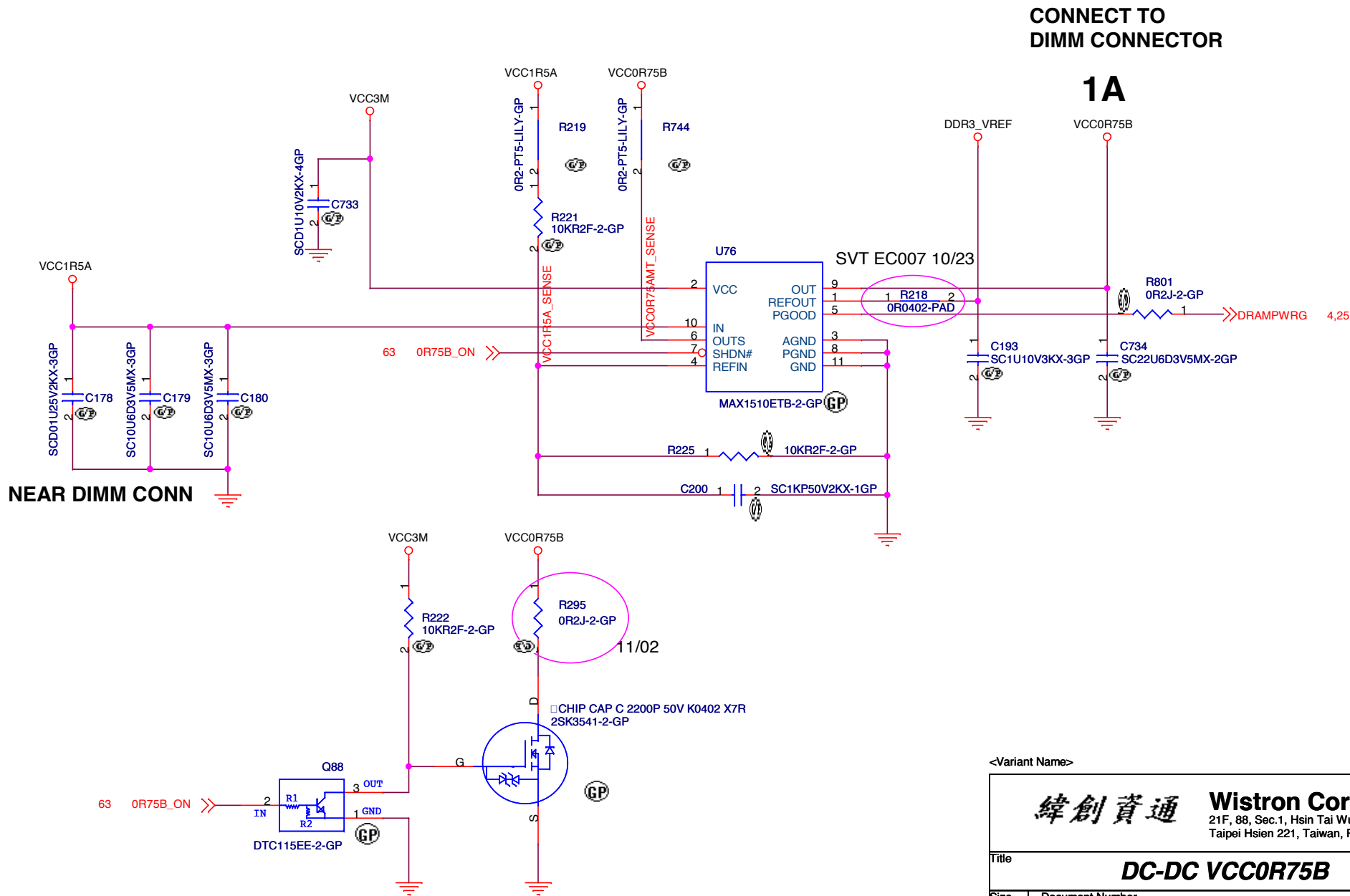
Rev
SC

Date: Monday, November 02, 2009

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DC-DC VCC0R75B

Size
A4

Document Number

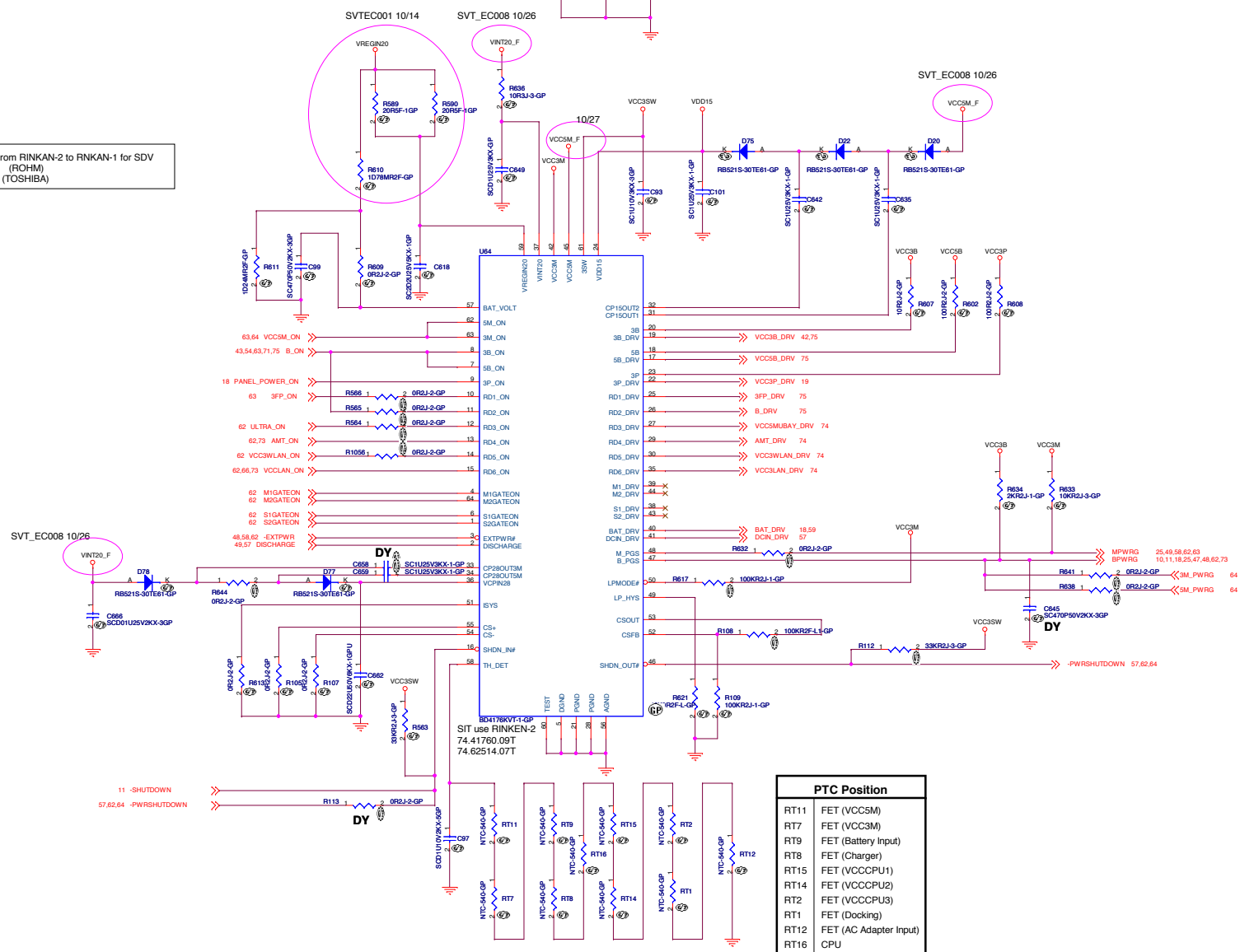
N-Note 3.0

Rev
SC

Date: Tuesday, November 03, 2009

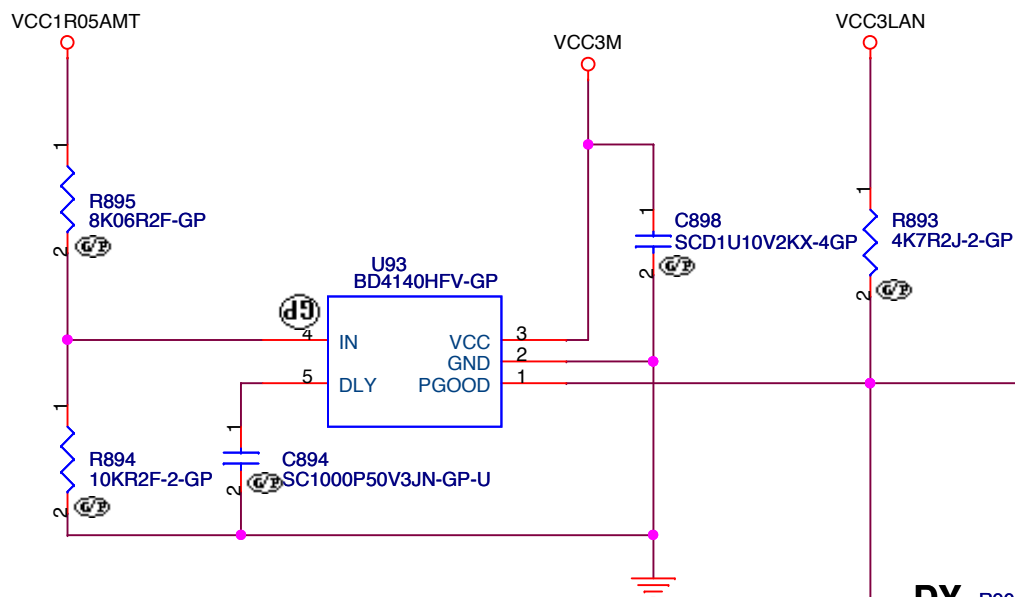
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Change U64 from RINKAN-2 to RNKAN-1 for SDV
- BD4176KVT (ROHM)
- TB62513FG (TOSHIBA)



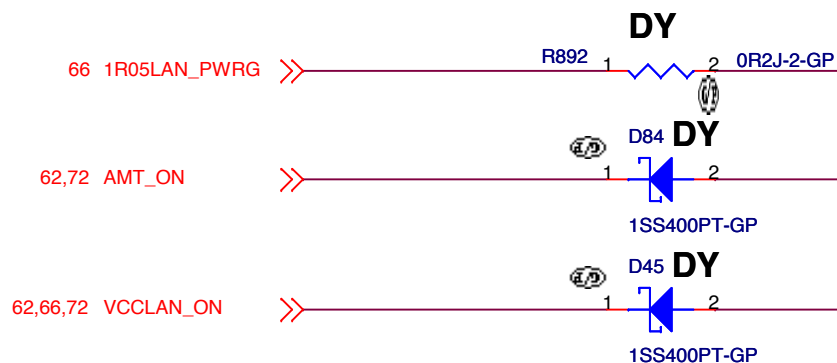
To add a PTC just near CPU thermal sensor (U79) and CPU.

PTC Position	
RT11	FET (VCC5M)
RT7	FET (VCC3M)
RT9	FET (Battery Input)
RT8	FET (Charger)
RT15	FET (VCCCPU1)
RT14	FET (VCCCPU2)
RT2	FET (VCCCPU3)
RT1	FET (Docking)
RT12	FET (AC Adapter Input)
RT16	CPU



AMT	YES	NO
U93	ASM	NO_ASM
R895	ASM	NO_ASM
R894	ASM	NO_ASM
C894	ASM	NO_ASM
C898	ASM	NO_ASM
R893	ASM	NO_ASM
R892	NO_ASM	NO_ASM
D84	NO_ASM	NO_ASM
D45	NO_ASM	NO_ASM
R909	NO_ASM	ASM

Logic



<Variant Name>

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

MEPWRG

Size
A

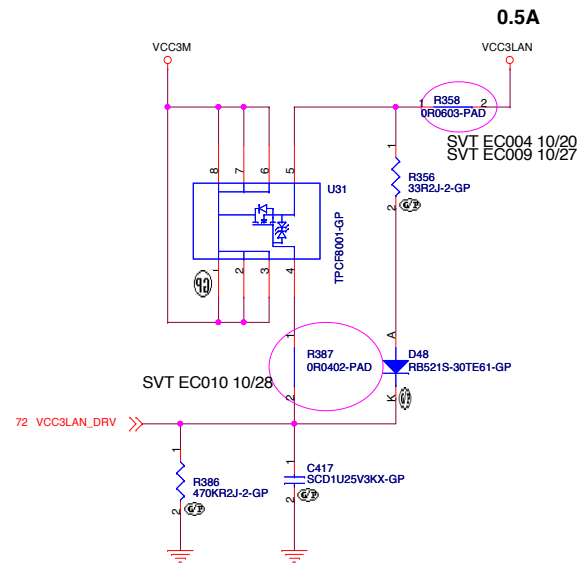
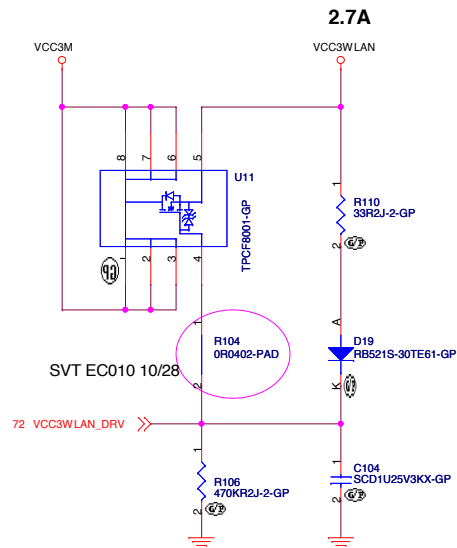
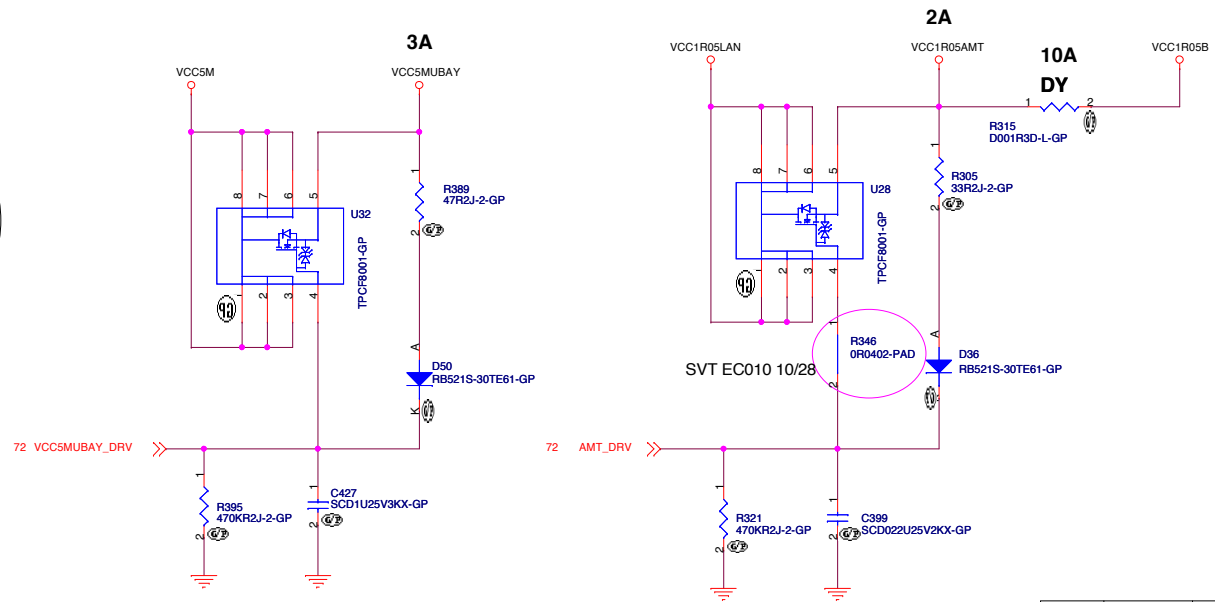
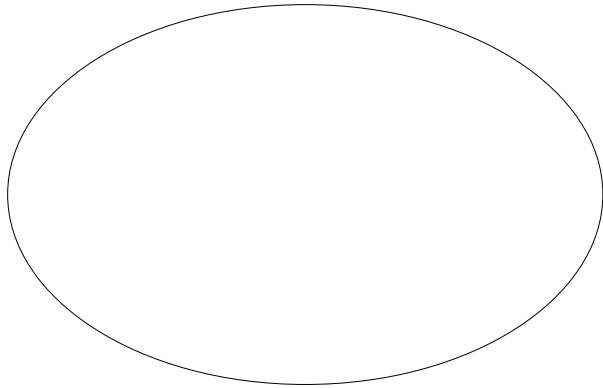
Document Number

N-Note 3.0

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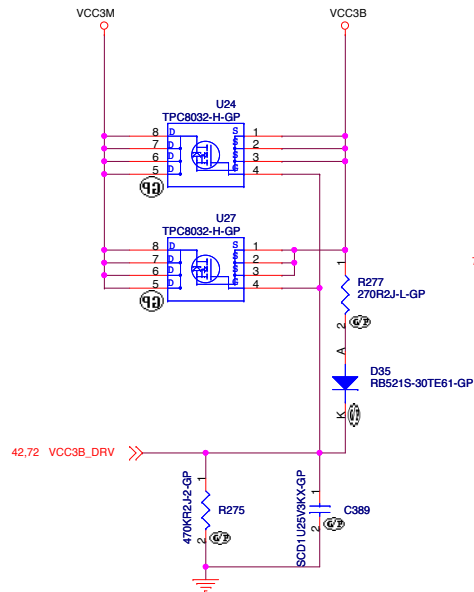
AMT	YES	NO
U28	ASM	NO_ASM
R305	ASM	NO_ASM
D36	ASM	NO_ASM
R346	ASM	NO_ASM
C399	ASM	NO_ASM
R321	ASM	NO_ASM
R315	NO_ASM	ASM

Logic

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
LOAD SW 1		
Size A3	Document Number N-Note 3.0	Rev SC
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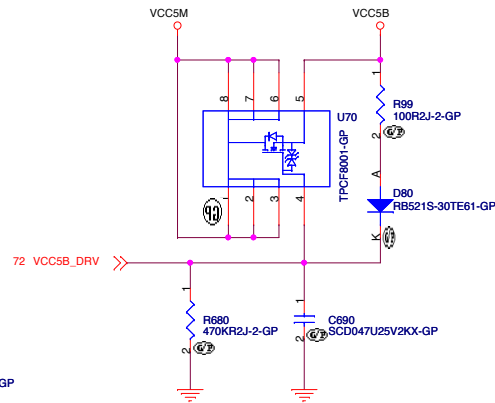
12A



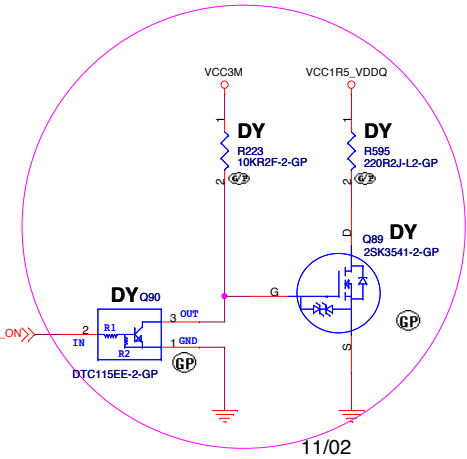
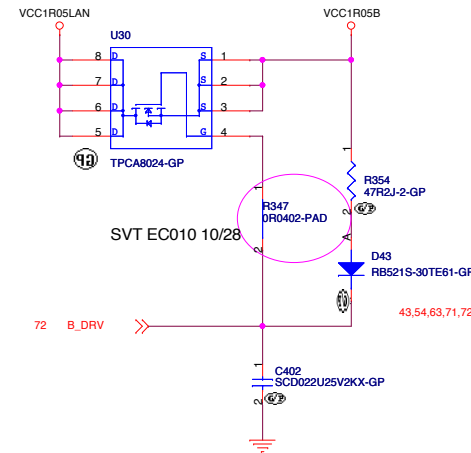
Table

ALWAYS ON	WWAN	NONWWAN
U24	ASM	NO_ASM

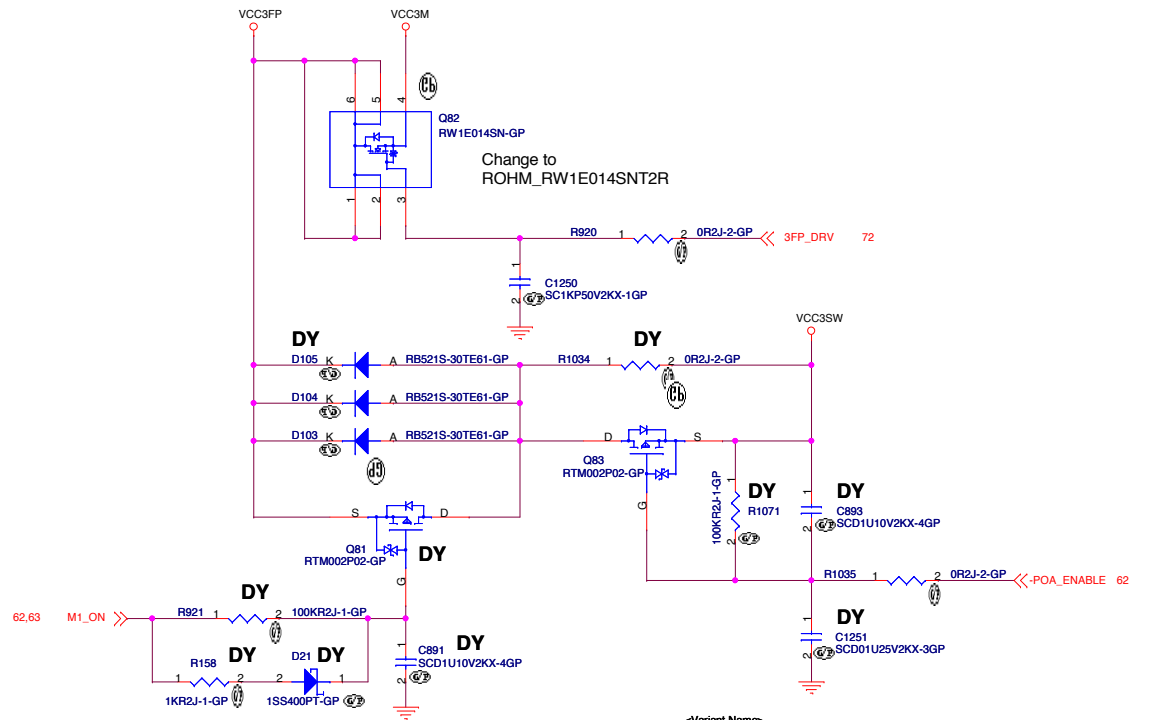
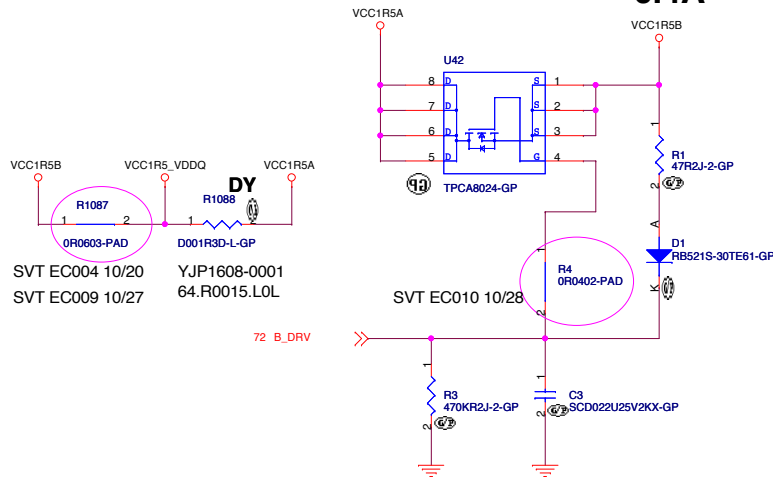
4A



6A



6.4A



<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

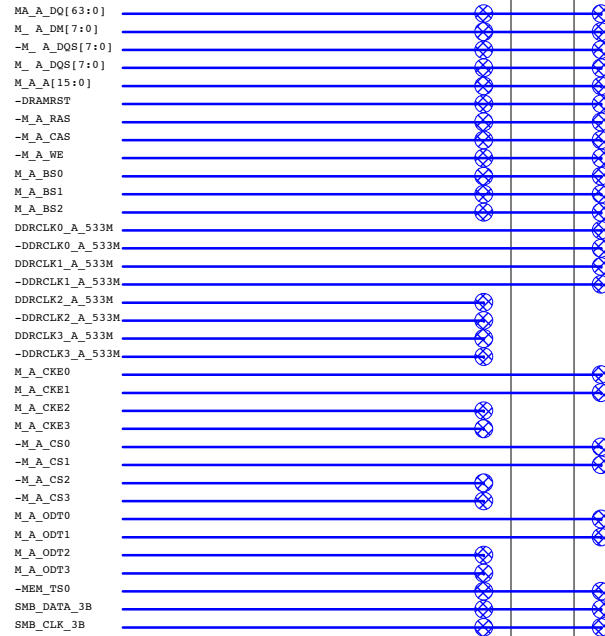
LOAD SW 2		
Size A3	Document Number	Rev SC
N-Note 3.0		
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SODIMM should be installed on CH0 Primary at first.

From Clarksfield

SODIMM CH-A Secondary

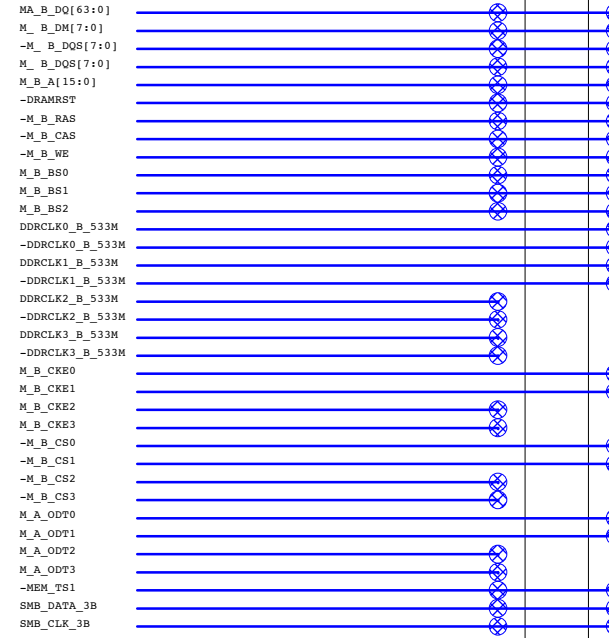
SODIMM CH-A Primary



From Clarksfield

SODIMM CH-B Secondary

SODIMM CH-B Primary



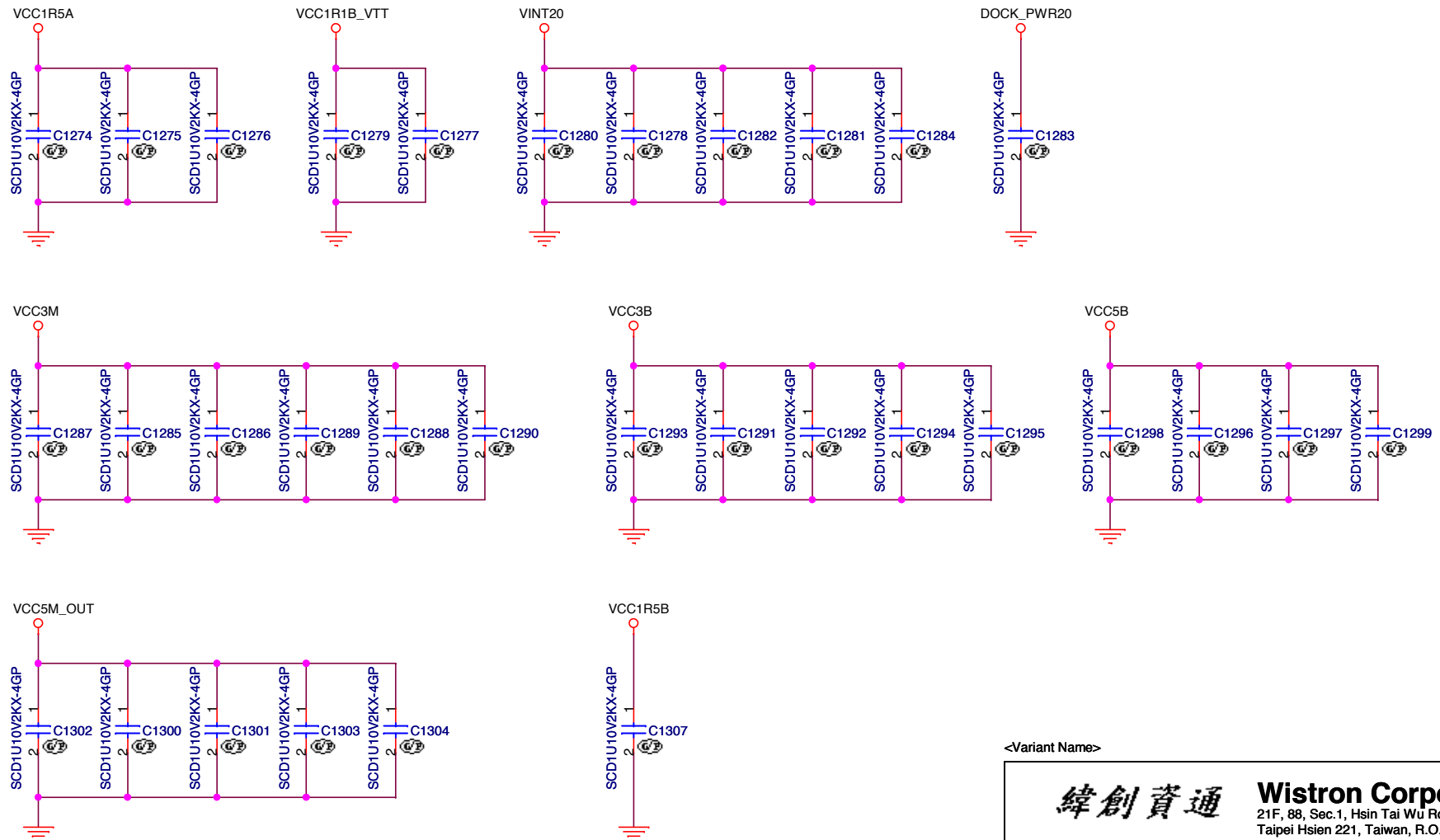
SODIMM IIC Address :
CH-A Primary : 50h
CH-B Primary : 51h
CH-A Secondary : 52h
CH-B Secondary : 53h

Pin1 on SODIM connector (VREF_DQ) only connects to DDR Voltage divider.
Clarksfield H17/J17 is left.

<Variant Name>

緯創資通		Wistron Corporation	
21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 305, Taiwan, R.O.C.			
File			
SODIMM CONFIGURATION			
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Long power trace EMI decoupling caps



<Variant Name>

緯創資通

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Title

EMI DECOUPLING

Size
A4

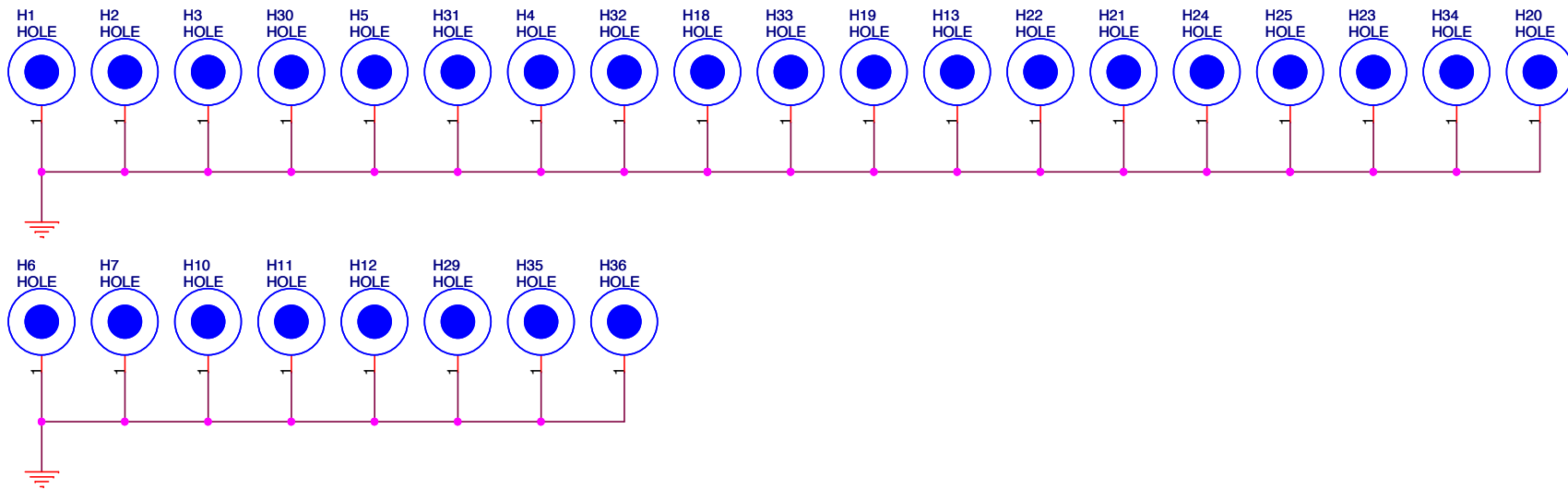
Document Number

N-Note 3.0

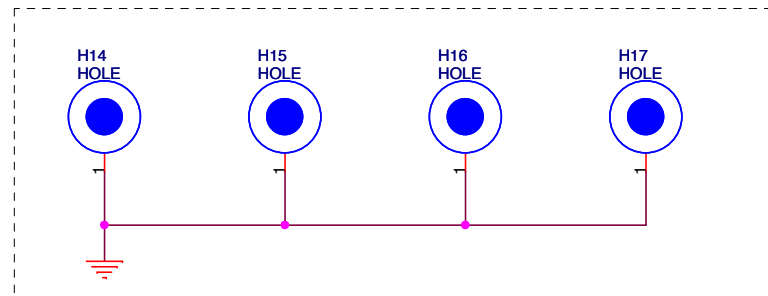
Rev
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Date: Monday, November 02, 2009

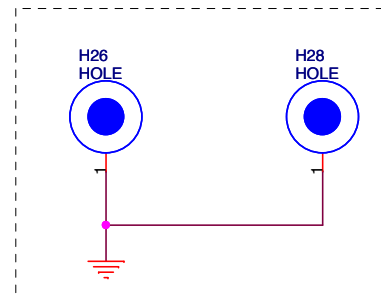
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BOSS for PCI Express H = 2.8mm
P/N:34.4B502.001

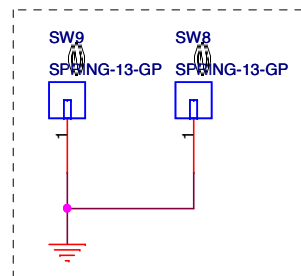


MB MXM BOSS H = 2.7mm
P/N:34.4Y909.001

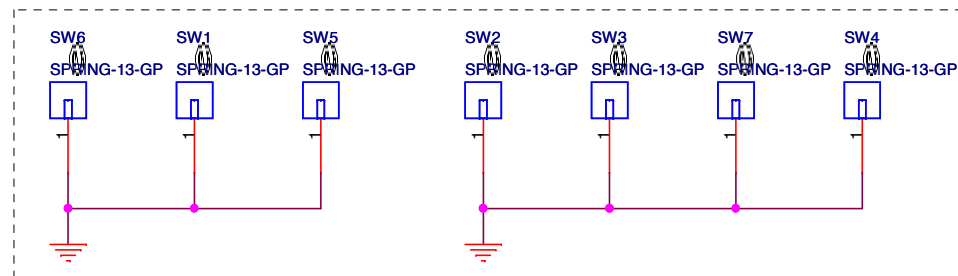


EMI STOPS


Bottom Side
P/N:34.13B01.001



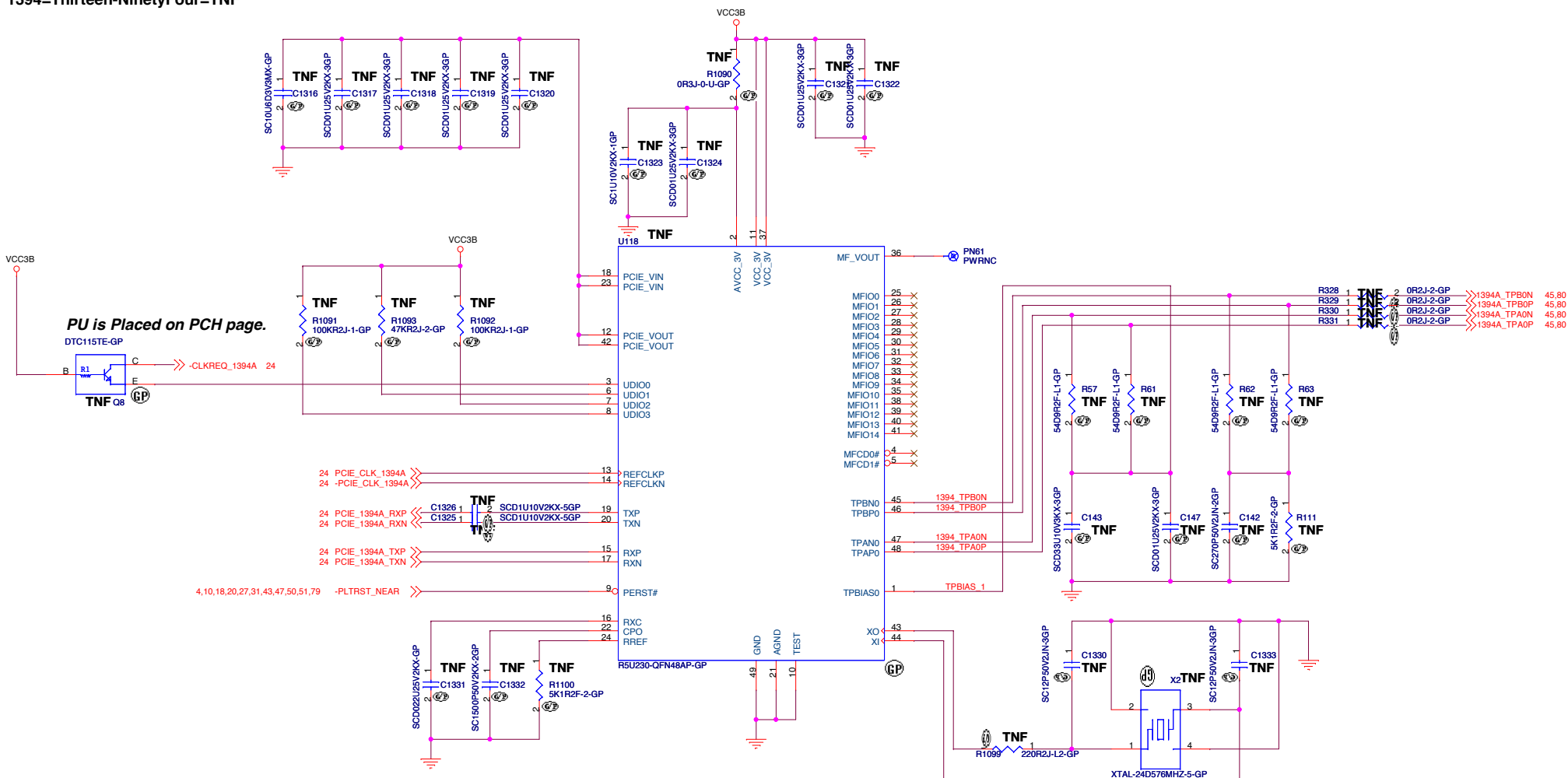
Top Side
P/N: 34.43E24.001



<Variant Name>

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Title			
HOLES/GND/PADS			
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Richo Recommended Conditions:
 Normal Frequency: 24.576MHz
 Frequency Tolerance: +/- 50ppm.
 Load Capacitance: 10pF.
 Effective Series Resistance: 50-ohm.
 Effective Shunt Capacitance: 7pF.

KDS Recommended Conditions:
Normal Frequency: 24.576MHz
Frequency Tolerance: +/- 30ppm.
Load Capacitance: 12pF+/-0.2.
Effective Series Resistance: 50-ohm.
Effective Shunt Capacitance: 7pF.

<Variant Name>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	

1394A CONTROLLER

Size

	Document Number
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Nico-

Rev

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